

DESIGN AND IMPLEMENTATION OF A DIRECT-SEQUENCE
SPREAD SPECTRUM WIRELESS MODEM

BY

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TABLE OF CONTENTS

CHAPTER	PAGE
1 INTRODUCTION	1
2 DESIGN OVERVIEW	4
2.1 Design Objectives	4
2.2 Determination of Design Parameters	5
3 TRANSMITTER AND RECEIVER ARCHITECTURE	7
3.1 Elements of Digital Communication	7
3.2 Modulation in the Transmitter	8
3.3 Spectrum Spreading in the Transmitter	9
3.4 Spectrum Despreading in the Receiver	10
3.5 Demodulation in the Receiver	15
4 DESIGN IMPLEMENTATION	18
4.1 Outline of Design Implementation	18
4.2 Transmitter Implementation	18
4.3 Receiver Implementation	21
4.4 Local Oscillator and Clock Designs	27
5 SYSTEM PERFORMANCE	30
5.1 Transmitter Performance	30

5.2 Receiver Performance	32
6 CONCLUSIONS.....	35
APPENDIX A LINK BUDGET ANALYSIS.....	37
APPENDIX B SCHEMATIC DIAGRAMS	40
APPENDIX C RADIO DESIGN CONSIDERATIONS	54
REFERENCES	56

CHAPTER 1

INTRODUCTION

With the rapidly growing number of people wanting to keep in touch at all times and from all locations, the demand for wireless communication systems is expanding. The wireless communication market has been growing at an annual rate of 17% since 1984, and the popularity of cellular telephones, pagers, and wireless computer networks continues to increase [1]. In response to demand for additional frequency allocations for wireless communication systems, the Federal Communications Commission (FCC) has authorized the use of unlicensed spread spectrum communication systems in several of the industrial-scientific-medical (ISM) frequency bands [2]. Many companies have already introduced new products -- such as cordless telephones, baby monitors, and wireless computer networks -- operating in these bands. In this project, we explore the design and implementation of an unlicensed medium-rate wireless modem utilizing spread spectrum transmission and reception in the 902-928 MHz ISM band.

In addition to being authorized for unlicensed use in several frequency bands, spread spectrum systems offer several technical advantages over traditional radio systems. For example, spread spectrum systems can provide resistance to interference (both unintentional and intentional) [3], resistance to signal distortions caused by the radio environment [4], and the ability to support multiple users in the same frequency band

(multiple access) [5]. These advantages can be important in the crowded electromagnetic spectrum, often allowing a spread spectrum radio to operate where interference and signal distortions disrupt non-spread spectrum communication systems [3]. While spread spectrum systems offer these enticing benefits, the advantages come at the price of increased cost and complexity. For example, the larger bandwidth of a spread spectrum system may require a more expensive radio frequency (RF) section in both the receiver and transmitter. In addition, a spread spectrum receiver requires methods to achieve and maintain synchronization to the incoming signal. Balancing performance and cost issues is a key task for the systems engineer when designing a new communications system.

The purpose of this project is to explore the basic architecture and implementation of a spread spectrum radio modem. Spread spectrum systems are traditionally classified as either frequency hopping (FH) or direct-sequence (DS). In frequency hopping systems, data bits are transmitted on a number of different frequencies. The transmitter switches from one frequency to another based on a predetermined pattern, changing frequencies either once every few bits (slow hop) or multiple times per bit (fast hop). As the transmitter hops, the spectrum of the transmitted signal is spread over a much larger range than would be required by a traditional modulation scheme. In direct-sequence spread spectrum (DS-SS) systems, each data bit is modulated by a higher-rate bit stream, known as the spreading sequence or spreading code. When the source data bits are modulated by the spreading sequence, the resulting spectrum will be spread by the ratio of the clock rate of the spreading sequence to the clock rate of the data sequence. While both forms of spread spectrum have their advantages and disadvantages, DS-SS systems make fewer demands on the radio frequency section of the system, and as a result, will be used in this project.

The design objective is to create a basic but fully functional DS-SS radio modem.

Developing this modem will provide insight into the implementation details of a DS-SS transmitter and receiver. It will also offer the opportunity to learn about designing and constructing RF circuitry. The system level issues involved in the architectural decisions about the modem will also be addressed. The next chapter outlines the specific objectives and the design parameters of the modem to be created. Chapter 3 outlines the architecture of a DS-SS system, and the implementation developed for this project is presented in Chapter 4. Chapter 5 reports the performance results obtained for the complete system. Finally, Chapter 6 presents the conclusions and suggestions for further work.

CHAPTER 2

DESIGN OVERVIEW

2.1 Design Objectives

The project objectives are to design and build a spread spectrum transmitter and receiver. Using a synchronous or asynchronous interface, data supplied to the transmitter will be spread spectrum modulated onto an RF carrier, amplified, and transmitted. The receiver will acquire the spread spectrum signal, track the variations in the transmitter carrier frequency and spreading sequence, and demodulate the data. The performance goals of the system are

1. To support a data rate of at least 57,600 bits per second.
2. To operate over an indoor radio environment -- such as an office -- up to 100 feet and over an outdoor line-of-sight environment up to 500 feet.
3. To meet FCC requirements for unlicensed operation in the 902-928 MHz industrial-scientific-medical (ISM) band. A summary of the FCC requirements is shown in Table 2.1.

Table 2.1. FCC Part 15 Requirements for Unlicensed Operation 902-928 MHz [2].

Maximum bandwidth	902-928 MHz
Minimum bandwidth	500 kHz (6 dB bandwidth)
Out-of-band emissions	The radio frequency power in any 100 kHz band outside the 902-928 MHz range must be 20 dB below the highest 100 kHz band within the 902-928 MHz range.
Power spectral density	Maximum of 8 dBm within any 3 kHz bandwidth
Maximum power	30 dBm (1 W)
Processing gain	10 dB minimum

2.2 Determination of Design Parameters

For the design objectives presented, many implementations are possible. In order to limit the scope of the design and meet the stated objectives, a set of parameters must be defined. These parameters include the system data rate, transmitter power level, the modulation method, and spectrum spreading parameters.

2.2.1 Data rate

To meet the data transmission rate objective, the modem will transmit and receive at 100,000 bits per second (100 kbps). To limit the complexity of the design, no channel coding will be provided – the user data will be transmitted directly with no error detection or correction codes.

2.2.2 Modulation method

To limit the complexity of the design, the modulation method will be based on binary phase shift keying (BPSK).

2.2.3 Transmitter Power

The transmitter will have an output power of at least 10 dBm (10 mW) and not more than 30 dBm (1 W). The minimum power level is established by the receiver sensitivity and the maximum range desired; a detailed analysis is shown in

Appendix A. The maximum transmitter power is limited to 1 W by the FCC regulations (see Table 2.1). The design will target a transmitter power of 15 dBm.

2.2.4 Spectral Spreading

The FCC requirements mandate a processing gain of at least 10 dB. For a data rate of 100 kbps, a minimum spreading code rate of 1 Mcps (million chips per second) is needed. A spreading code of 128 chips per bit will be used in this project, resulting in a system chip rate of 12.8 million chips per second (Mcps). The chip rate will provide a processing gain of 21.07 dB, the maximum processing gain possible given the bandwidth limits of the ISM band and the desired data rate.

2.2.5 Carrier Frequency

The carrier frequency will be 915.000 MHz, the center of the 902-928 MHz ISM band. With the given carrier frequency and processing gain of the system, the transmitted signal will occupy most of the ISM band, assuming BPSK modulation. Some filtering will be necessary to restrict modulation products to acceptable levels outside the ISM band.

CHAPTER 3

TRANSMITTER AND RECEIVER ARCHITECTURE

3.1 Elements of Digital Communication

The goal of the modem is to transmit a sequence of symbols, B_k , over a channel as shown in Figure 3.1. The symbols are either '0' or '1', representing the bits of either a digitally sampled analog signal or other user-provided digital data. From the symbols B_k , the transmitter generates a signal $y(t)$ that propagates over a channel, such as an indoor or outdoor radio environment. The channel shown in Figure 3.1 is a very simple radio environment (representing an indoor or outdoor environment only under the most favorable conditions), but three key elements of a radio environment are present: The channel delays the signal by τ_p , attenuates the signal by a factor of L , and adds a noise signal $n(t)$. For the purposes of this project, the delay τ_p represents the propagation time of the signal traveling from the transmitter to the receiver. The delay τ_p is assumed to be constant or very slowly changing. The attenuation factor L represents the loss of signal strength due to distance and other factors of the radio environment, and like τ_p , is assumed to be constant or slowly changing. The noise signal $n(t)$ is assumed to be additive white Gaussian noise (AWGN). The function of the receiver is then to find an estimate, \hat{B}_k , of the original B_k based on the received signal $y(t - \tau_p) / L + n(t)$.

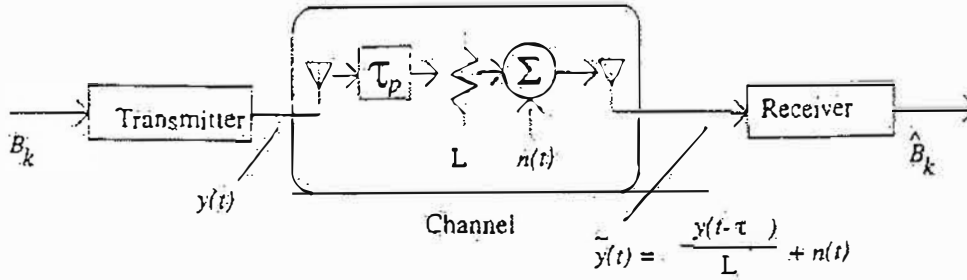


Figure 3.1 A Digital Communication System Model

3.2 Modulation in the Transmitter

The function of the transmitter is to encode the symbols B_k onto a radio frequency (RF) carrier for transmission. While there are a variety of modulation methods available for digital transmission [5]-[8], one of the simplest is binary phase shift keying (BPSK). In BPSK, the phase of a carrier signal is shifted by 0 or π depending on the value of the bit B_k being transmitted. The result of BPSK modulation of a carrier signal at a radian frequency ω_0 by bits B_k of duration T can be represented by

$$s(t) = A \cos(\omega_0 t + \phi(t)), \quad (3.1)$$

where $\phi(t) = \pi B_k$ for $kT \leq t \leq (k+1)T$.

Alternatively, (3.1) can be written

$$s(t) = A b(t) \cos(\omega_0 t), \quad (3.2)$$

where $b(t) = (-1)^{B_k}$ for $kT \leq t \leq (k+1)T$.

If the data bits are essentially random with equal probability of being 0 or 1, then the one-sided power spectral density (PSD) of (3.2) can be shown [5] to be:

$$S_s(f) = A^2 \text{sinc}^2((f - f_0)T). \quad (3.3)$$

A plot of the power spectral density of $s(t)$ is shown in Figure 3.2. From Figure 3.2, it can be seen that most of the signal energy lies between $f_0 - 1/T$ and $f_0 + 1/T$ (where $1/T$ is the symbol rate). For purposes of comparison, the signal bandwidth can be approximated as the null-to-null spacing shown in Figure 3.2 as $2/T$, or twice the symbol rate.

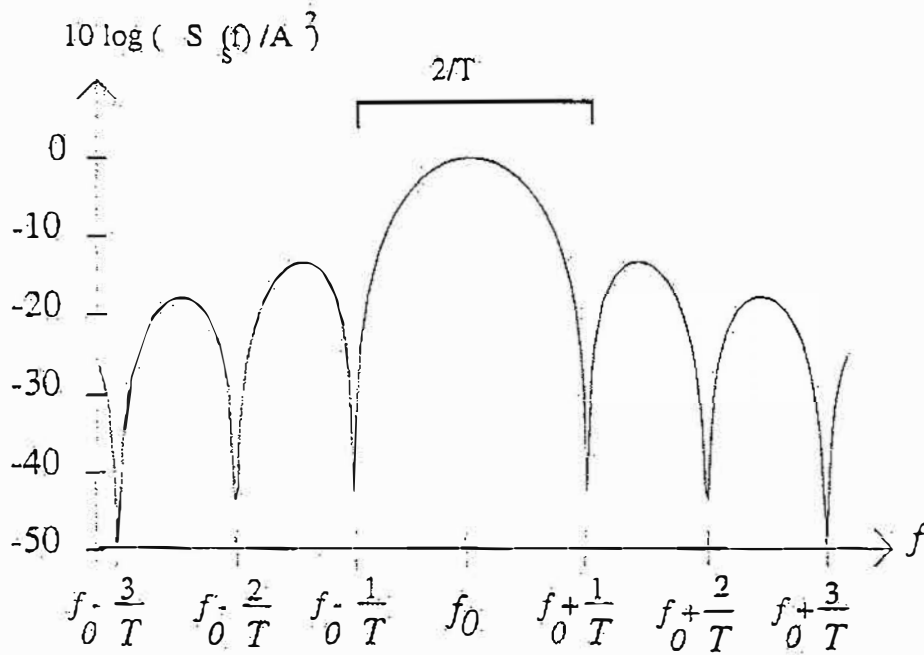


Figure 3.2 The Power Spectral Density of a BPSK Signal.

3.3 Spectrum Spreading in the Transmitter

In a DS-SS system, the transmitted signal $y(t)$ is created by multiplying the modulated signal $s(t)$ by a spectral spreading code $c(t)$ as shown in Figure 3.3. This can be written as

$$y(t) = c(t)s(t) = Ac(t)b(t)\cos(\omega_0 t), \quad (3.4)$$

with $b(t)$ as defined as for (3.2) and $c(t) = (-1)^{C_n}$ for $mT_c \leq t \leq (m+1)T_c$.

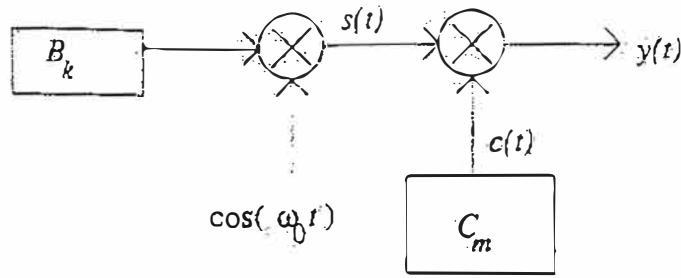


Figure 3.3 A DS-SS Modulator.

The sequence C_m (or signal $c(t)$) is referred to as the *spreading code*. Each symbol, C_m , of the spreading code has a duration of T_c seconds where $T_c \ll T$. There are many options for the choice of C_m , and a common choice of C_m is from the family of pseudo-noise (PN) sequences. These sequences have statistical properties that resemble a white-noise random process. One particular group of PN sequences, the *m*-sequences, is a group of linear sequences with well-understood statistical properties [5], [6], [9]. If C_m is an *m*-sequence, then the one-sided PSD of $y(t)$ is given by

$$S_y(f) = A^2 \text{sinc}((f - f_0)T_c). \quad (3.5)$$

Comparing $S_y(f)$ with $S_s(f)$, it is clear that the bandwidth of the spread signal $y(t)$ has been spread by a factor T/T_c compared to $s(t)$. This increase in bandwidth is called the *processing gain* of the system [5].

3.4 Spectrum Despreading in the Receiver

The function of the receiver shown in Figure 3.1 is to recover the symbols B_k from the incoming RF signal $\tilde{y}(t)$, where

$$\tilde{y}(t) = \frac{1}{L} y(t - \tau_p) + n(t). \quad (3.6)$$

Because of the unknown (and often time-varying) delay τ_p , loss L , and the noise $n(t)$ introduced in the channel, the output of the receiver is only an estimate \hat{B}_k . In a DS-SS system, the process of finding \hat{B}_k can be divided into two main steps. The first step is to despread the received signal. The output of the despreading operation is a non-spread spectrum radio signal that is processed in the second step of the receive process, demodulation, to yield the estimate of B_k .

Conceptually, the despreading operation is straightforward. If the exact delay τ_p were known, the receiver could multiply the received signal $\tilde{y}(t)$ by a copy of $c(t)$ delayed by τ_p , to obtain a signal $r(t) = \tilde{y}(t)c(t - \tau_p)$. Substituting for $\tilde{y}(t)$ and using the fact that $[c(t)]^2 = 1$,

$$\begin{aligned} r(t) &= \left[\frac{1}{L} \tilde{y}(t - \tau_p) + n(t) \right] c(t - \tau_p) \\ &= \frac{A}{L} c(t - \tau_p) c(t - \tau_p) b(t - \tau_p) \cos(\omega_0(t - \tau_p)) + n(t) c(t - \tau_p) \\ &= \frac{A}{L} b(t - \tau_p) \cos(\omega_0(t - \tau_p)) + n(t) c(t - \tau_p). \end{aligned} \quad (3.7)$$

If $n(t)$ is AWGN, then $n(t)c(t - \tau_p)$ will also be AWGN. Once the signal has been despread, the process of finding \hat{B}_k is then that of demodulating BPSK in AWGN. There are many methods of demodulating BPSK signals [5]-[8], and the specific architecture used in this project will be presented in Section 3.5. First, though, the process of despreading the received signal will be discussed.

The challenge in designing the despreading portion of a DS-SS receiver is to derive an estimate of τ_p , $\hat{\tau}_p$. In practical applications, the despreading task is usually divided into two subproblems. First, the receiver finds an initial estimate that is close to τ_p , usually

within half a chip duration (so $|\hat{\tau}_p - \tau_p| \leq \frac{T_c}{2}$). This process is called *acquisition*. Second, the receiver adjusts $\hat{\tau}_p$ to bring it closer to τ_p and keep $|\tau_p - \hat{\tau}_p|$ small. Over time, the value of τ_p will vary due to the relative motion of the transmitter and receiver, changes in the propagation environment, and drift and errors in the transmitter and receiver timing circuits. This process of improving and maintaining an accurate estimate $\hat{\tau}_p$ is called *tracking*.

3.4.1 Acquisition

A number of methods have been developed for acquiring the spreading sequence delay, τ_p . Several of the least complex techniques are classified as serial-search synchronization techniques. The receiver starts with one value for $\hat{\tau}_p$, attempts to despread the incoming signal at that trial value for $\hat{\tau}_p$, calculates a decision statistic, and then either adjusts $\hat{\tau}_p$ and continues the search or terminates the search with $\hat{\tau}_p$ as the estimate of τ_p . The estimate $\hat{\tau}_p$ can be adjusted in either discrete steps (typically 1/2 or 1/4 of T_c), or the frequency of the clock generating the local $c(t)$ can be offset, resulting in a constant linear variation in $\hat{\tau}_p$. Systems calculating a decision statistic over a fixed period of time are called *single-dwell* serial systems, and systems that perform a sequence of tests of increasing length to quickly rule out unlikely estimates of τ_p are called *multiple-dwell* serial systems [5].

The serial search techniques have the disadvantage of requiring a relatively large amount of time to operate. In particular, if either the spreading sequence is very long or if the range of values for τ_p is very large, then the synchronization process can be very time consuming. Other techniques offer improved synchronization speed. For example, a matched filter can achieve very fast synchronization [10] and [11], although implementing matched filters is not always feasible. Under medium to high signal-to-noise ratio conditions, it may be possible to detect the individual spreading chips directly, a technique

used in *rapid acquisition by sequential estimation* (RASE) and *recursion-aided RASE* (RARASE) techniques [5]. Some parallel methods for calculating $\hat{\tau}_p$ have also been studied [12], [13].

The relatively short spreading code used in this project allows a serial search to complete in a timely fashion; as a result, the multiple-dwell serial search with steps of $T_c / 2$ provides satisfactory results with minimum complexity.

3.4.2 Tracking

Once an initial estimate of $\hat{\tau}_p$ has been found, the receiver must track the received spreading sequence to improve the estimate and respond to variations in τ_p . The basic method used for tracking the spreading sequence is called a delay-lock loop (DLL), as shown in Figure 3.4.

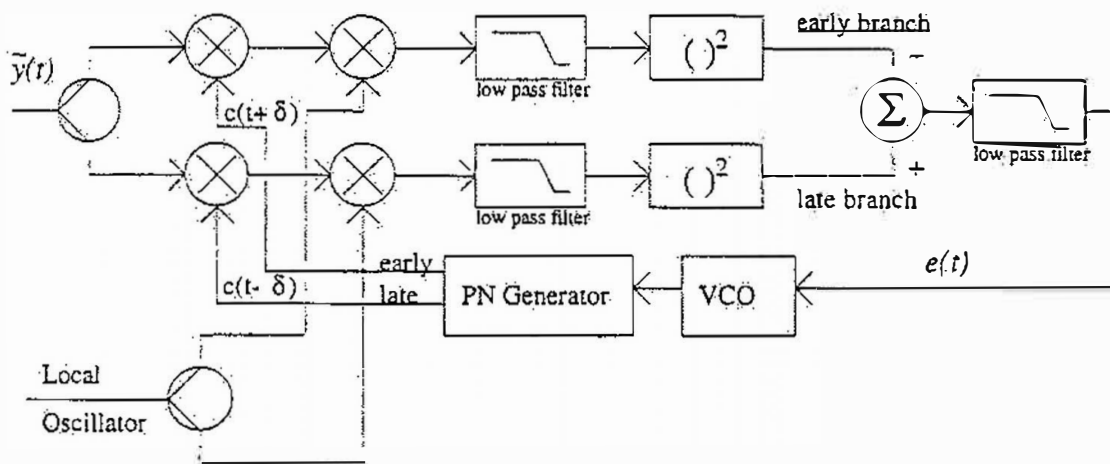


Figure 3.4 A Basic Delay-Lock Loop.

In essence, the DLL works by forming an error signal, $e(t)$, that is proportional to the difference between the current $\hat{\tau}_p$ and the actual τ_p . When the spreading sequence $c(t)$ is

from an m -sequence of length N , the autocorrelation of $c(t)$ is periodic with period NT_c .

From [6], the autocorrelation function of $c(t)$ is

$$R(\tau) = \begin{cases} -1 + \left| 1 - \frac{\tau}{T_c} \right| (N + 1) & \text{for } |\tau| \leq T_c \\ -1 & \text{for } T_c < \tau < (N - 1)T_c. \end{cases} \quad (3.8)$$

As can be seen in Figure 3.5, the value of the autocorrelation of $c(t)$ varies from -1 for a delay of T_c or greater up to a maximum of N when the delay is zero. In the DLL, the early and late PN sequences are offset by equal fractions of T_c from the main, on-time PN signal. (The offset is shown as δ in Figure 3.4, and often $\delta = T_c / 2$.) If the PN sequence in the receiver is precisely synchronized with the incoming signal, then the early and late branches will have equal outputs. If the receiver code estimate is early ($\hat{\tau}_p < \tau_p$), then the output from the early branch will be less than for the late branch. If the receiver code estimate is late ($\hat{\tau}_p > \tau_p$), then the output from the early branch will be greater than the late branch. By subtracting the early branch output from the late branch output, an error signal $e(t)$ is generated, indicating the direction in which to adjust the voltage controlled oscillator (VCO) to bring the local code sequence into precise alignment with the received signal.

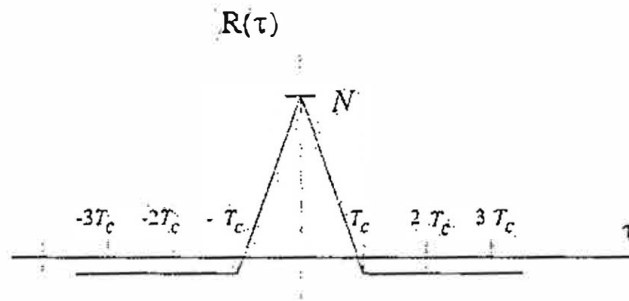


Figure 3.5 Autocorrelation Function of an M -Sequence.

The two main problems with the DLL are the complexity and the sensitivity to gain imbalance in the two branches [5]. The complexity results from the use of two complete despreading and downconversion branches, and any gain imbalance between the two branches causes an offset in the error signal, $e(t)$. A somewhat simpler tracking loop that avoids these problems is the tau-dither loop. Instead of computing the early and late correlation values simultaneously, the tau-dither loop uses a single correlation branch and alternates (dithers) the PN sequence between the early and late values. The drawback is that the tau-dither loop has somewhat poorer theoretical performance than the DLL due to noise from the dithering process [6]. Another tracking system, the double-dither loop, solves both the noise problem of the tau-dither loop and the gain imbalance sensitivity problem of the delay-lock loop. The double-dither loop is basically a combined version of the two systems -- there are two correlation branches which alternate functioning as the early and late branches [6].

Despite the drawbacks to the basic delay lock loop, the basic DLL will be used in this project. Conceptually, it is straightforward, and the lack of a dithering process makes testing and adjusting the circuit easier. The details of the implementation and a method for compensating for the gain imbalance problem will be discussed in Chapter 4.

3.5 Demodulation in the Receiver

Once the receiver has despread the signal $\tilde{y}(t)$ to generate a BPSK signal $r(t)$, the data encoded on $r(t)$ must be demodulated. There are many methods for recovering BPSK data, and the references [5]-[8] can be consulted for additional information. For this project, differentially coherent demodulation was selected on the basis of providing reasonable performance with relatively low complexity. A block diagram for a differentially coherent demodulator is shown in Figure 3.6.

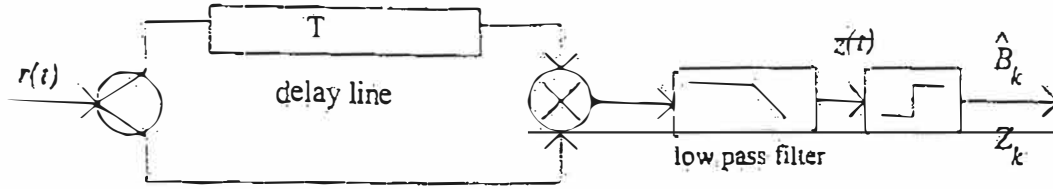


Figure 3.6 A Differentially Coherent Demodulator.

Let $d(t)$ represent the modulation present on the received signal $r(t)$ so that (neglecting noise), $r(t) = d(t) \cos(\omega_0 t)$. Then, as shown in Figure 3.6,

$$z(t) = r(t)r(t-T). \quad (3.9)$$

If the bit period T is equal to $\frac{2\pi N}{\omega_0}$ for some integer N , then (3.9) becomes

$$\begin{aligned} z(t) &= r(t-T) \\ &= d(t) \cos(\omega_0(t - \tau_p)) d(t-T) \cos(\omega_0(t-T - \tau_p)) \\ &= \frac{1}{2} d(t) d(t-T) \cos(\omega_0 T) + \frac{1}{2} d(t) d(t-T) \cos(\omega_0(2t - 2\tau_p - T)). \end{aligned} \quad (3.10)$$

Since $\cos(\omega_0 T) = \cos(\frac{\omega_0 2\pi N}{\omega_0}) = \cos(2\pi N) = 1$ and the double-frequency term is

essentially eliminated by the low-pass filter, (3.10) can be approximated as

$$z(t) \approx \frac{1}{2} d(t) d(t-T). \quad (3.11)$$

When a differentially coherent demodulator is used, the source data B_k must be differentially encoded prior to transmission so that it can be recovered from $r(t)$. For an input sequence B_k , let the transmitted sequence $D_k = B_k \oplus D_{k-1}$. If Z_k is the decoded symbol for $z(t)$ during $kT \leq t < (k+1)T$, then

$$Z_k = D_k \oplus D_{k-1} \quad (3.12)$$

Substituting for D_k , (3.12) becomes

$$Z_k = B_k \oplus D_{k-1} = B_k. \quad (3.13)$$

Thus, if the data bits are differentially encoded at the transmitter, the decoded data bits will be available at the output of the differentially coherent demodulator.

CHAPTER 4

DESIGN IMPLEMENTATION

4.1 Outline of Design Implementation

This chapter describes the implementation of the spread spectrum transmitter and receiver. Block diagrams show the high level implementation structure, and key elements of the design are explained. Complete circuit-level details are covered in the schematics in Appendix B. Although not discussed as part of the system architecture in Chapter 3, the control of timing and frequency in both the transmitter and receiver is an important implementation issue; these control circuits are described in this chapter with complete schematics in Appendix B. During the implementation of the transmitter and receiver, a number of items were found to play critical roles in the system design. These items, addressed during the project implementation, are listed in Appendix C.

4.2 Transmitter Implementation

As shown in Figure 4.1, the transmitter consists of the bit source, the spreading sequence generator, the modulator, the output filter, the RF amplifier, and the antenna. In actual use, the bit source could be data from a personal computer (PC) (for providing wireless, high-speed Internet access or other data services). The transmitter also includes two digital clocks and a 915.000 MHz RF local oscillator. The first digital clock, the

spreading sequence generator clock (chip clock), is used to generate the second clock, the data bit synchronizing clock (bit clock).

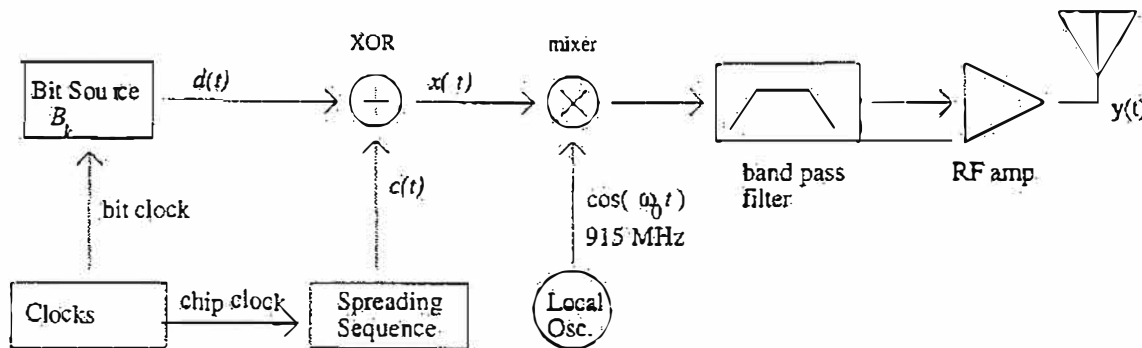


Figure 4.1 The Transmitter Top Level Block Diagram.

The bit source can be a test pattern or the user-supplied data as shown in Figure 4.2. The user-supplied data stream is an asynchronous serial signal (RS-232 compatible, for example) sampled by the bit clock for modulation and transmission. For the test pattern, a 127 bit sequence known to the receiver is transmitted. The bits to be transmitted, B_k , are differentially encoded as $D_k = B_k \oplus D_{k-1}$ (with D_{-1} arbitrarily set to 0) and used to generate the signal $d(t) = (-1)^{D_k}$ for $kT \leq t < (k+1)T$. A jumper is provided to switch the transmitter between user-data mode and test pattern mode.

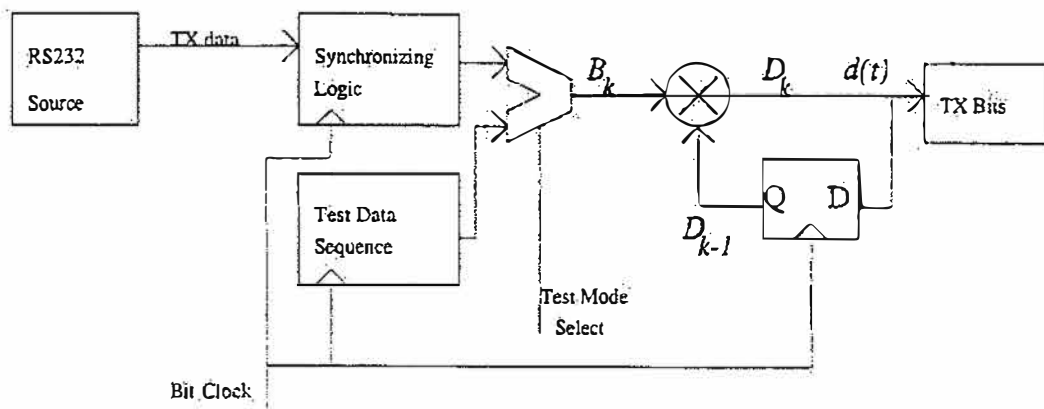


Figure 4.2 The Bit Source Generator.

The spreading signal $c(t)$ shown in Figure 4.1 is derived from the PN sequence C_m , with $c(t) = (-1)^{C_m}$ for $mT_c \leq t < (m+1)T_c$. The sequence C_m is created with an eight bit shift register that generates a 255 chip long m -sequence and additional logic that modifies the 255 chip sequence by duplicating the last bit, bringing the sequence length to 256. The block diagram for the PN generator is shown in Figure 4.3. The shift register shifts 255 times for every 256 clock cycles; the one non-shift interval causes the last bit to be repeated and results in a sequence that repeats every 256 clock cycles. The system chip rate is 128 chips per bit, so that there are two bits modulated with each repetition of the spreading sequence. The characteristic polynomial for the PN sequence used in this project is $x^8 + x^6 + x^5 + x^4 + 1$, selected from a table in [6].

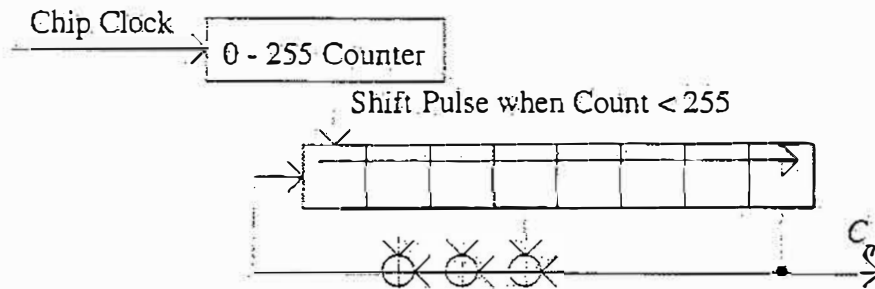


Figure 4.3 The PN Generator.

In the actual circuit, the baseband data signal $d(t)$ and the spreading signal $c(t)$ are combined digitally by modulo-2 addition (exclusive OR) of each data bit, D_k , with the successive bits of the PN sequence, C_m . The output of the PN modulator is a bit stream $x(t)$ switching at 128 times the rate of $d(t)$. For a 100 kbps bit rate, the chip rate is 12.8 Mcps. This high-rate bit stream, $x(t)$, is used to modulate the 915.000 MHz RF carrier. As shown in Figure 4.1, the output of the upconversion mixer is bandpass filtered to remove unwanted harmonics and limit the signal energy to the allowed 902-928 MHz band. The output from the filter is amplified and sent to a quarter-wavelength monopole antenna.

As shown in Appendix B, the transmitter is implemented in a mix of analog and digital circuits. The test data sequence, multiplexor, PN generators, and differential encoder are implemented in a digital design in a field programmable gate array (FPGA), the XC3064A manufactured by Xilinx. The design was created in VHDL* and synthesized into gate-level logic with the Synopsys FPGA Compiler. Finally, Xilinx XACT software was used to place and route the gate-level logic for loading into the XC3064A FPGA. The analog portions of the design consist of a doubly balanced diode mixer used to modulate the data onto the 915.000 MHz RF carrier, the bandpass filter, and the amplifier stages used to drive the antenna. The 915.000 MHz RF oscillator implementation is discussed in Section 4.4. Although not shown in the block diagram, the transmitter also includes a microcontroller for power-up configuration of the FPGA and diagnostic use.

4.3 Receiver Implementation

The receiver consists of an RF front-end, acquisition and tracking control, despreaders and downconverters, a demodulator, and a bit handler as shown in Figure 4.4. The RF front end amplifies the received signal $\tilde{y}(t)$ and splits it into three branches. Two branches of the RF signal are used by the delay lock loop (DLL), and the third branch is used by the demodulator. The DLL adjusts the system chip clock to follow variations in the transmitter spreading code clock. The demodulator serves two purposes. The main output from the demodulator is the estimate of the received data bits, \hat{B}_k . The other purpose of the demodulator is to provide a received signal quality estimate used by the acquisition and tracking module.

* VHDL stands for VHSIC (very high speed integrated circuit) Hardware Description Language, a high-level language for describing digital circuits. See [14] for additional information on VHDL.

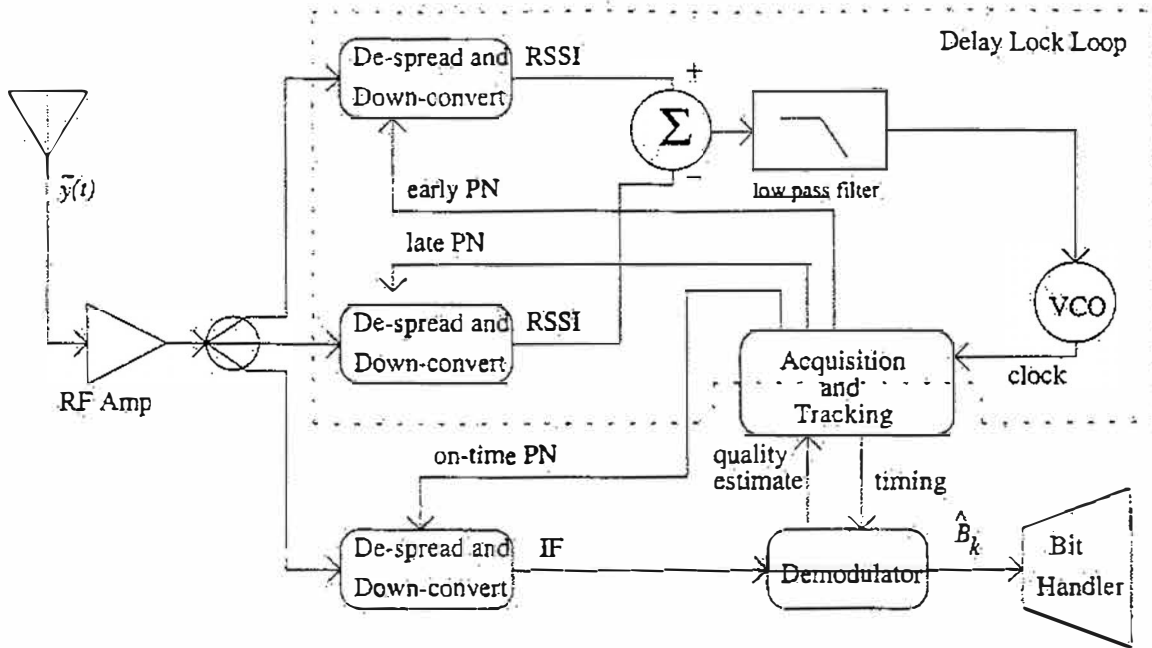


Figure 4.4 The Receiver Top-Level Block Diagram.

4.3.1 Despreader and down converter

The receiver implementation shown in Figure 4.4 uses three despreading/downconverter modules. The block diagram for the despreader/downconverter module is shown in Figure 4.5. The three despreading modules operate identically, each using the same PN sequence but with different delays. Two despreader/downconverter modules are used in the early and late branches of the DLL, and the third despreader/downconverter module generates the signal for the demodulator. The first two modules despread the incoming signal with early and late versions of the local spreading sequence. After despreading, the signals are mixed with a 904.300 MHz local oscillator signal to downconvert to 10.7 MHz which is then filtered by a narrowband filter to provide selectivity. The output of the narrowband filter is supplied to an intermediate frequency (IF) amplifier, which has, as an output, a received signal strength indicator (RSSI) proportional to the logarithm of the input power to the amplifier. In this configuration, the RSSI gives the approximate correlation between the incoming signal and the supplied spreading sequence. The first

despreader module is supplied with a PN sequence that is one-half of a chip early ($\delta = +T_c / 2$) relative to the main branch, and the second despreader module is supplied a one-half chip late ($\delta = -T_c / 2$) PN sequence. By comparing the RSSI outputs from the two amplifiers, the tracking loop can adjust the chip clock VCO to equalize the RSSI values. When the early and late branches are equal, the main PN sequence is properly aligned with the received signal.

The third despreading module generates the signal for the demodulator. The received signal is despread with the on-time version of the local PN sequence and downconverted to a first IF of 10.7 MHz. The first IF signal is narrowband filtered and amplified by the IF amplifier at 10.7 MHz. The IF output from the amplifier is limited to about 0.3 V peak-peak swing, and this signal is downconverted again, this time to the final IF frequency of 400 kHz. The hard-limited 400 kHz signal is output to the demodulator for data recovery.

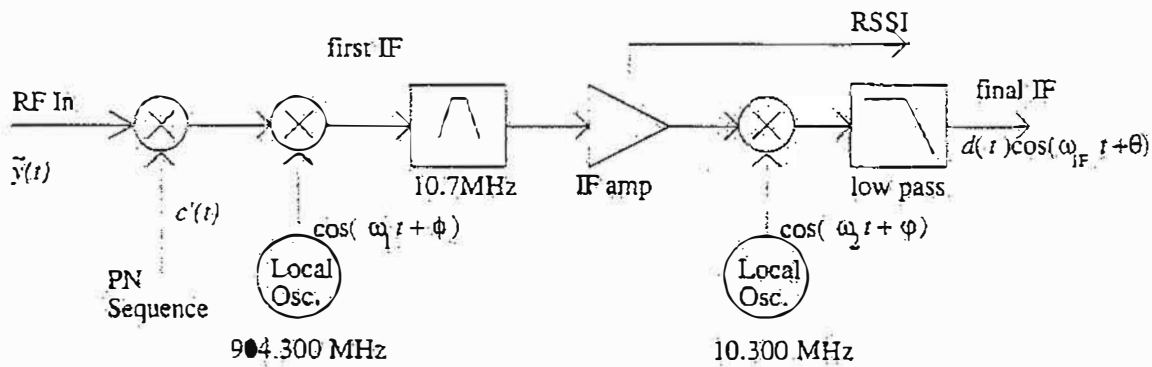


Figure 4.5 A Despreader and Downconverter Module.

The despreader/downconverter module functions are implemented with passive power splitters and doubly balanced diode mixers. The IF amplifier is the NE605 from Signetics. As configured in this circuit, the NE605 provides 70 dB of gain with a limiting output

stage and RSSI. The 904.300 MHz and 10.300 MHz local oscillators are described in Section 4.4.

4.3.2 Demodulator

The purpose of the demodulator is to estimate B_k from the 400 kHz final IF signal. In the transmitter, the data symbols are differentially encoded with binary phase shift keying. The demodulator, shown in Figure 4.6, samples each incoming symbol and uses it as a phase reference for decoding the subsequent symbol. In this project, the samples of the previous symbol are stored in a delay line implemented as a digital shift register. For the 400 kHz IF signal, the signal is sampled at 32 samples per cycle, resulting in a 12.8 MHz sampling rate. A 64 bit shift register stores two cycles of the 400 kHz IF as the phase reference for decoding the next symbol. (At the 100 kbps rate, two cycles at 400 kHz represent half of a symbol period. A larger shift register to store a complete symbol might produce higher performance for the demodulator, but the design was limited by the number of flip-flops available in the FPGA.) The output of the delay line is added modulo-2 (XOR) with the current incoming signal and summed in an accumulator. The output of the accumulator is used to make a bit decision and supply the quality estimate for the acquisition module.

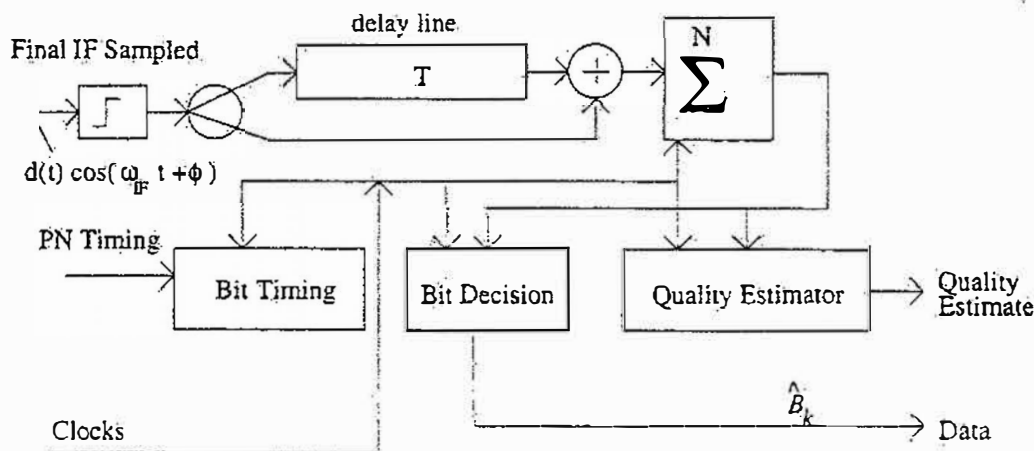


Figure 4.6 The Demodulator Block Diagram.

The demodulator is implemented in a Xilinx XC3064A FPGA. The design was created in VHDL and synthesized into gate-level logic with the Synopsys FPGA Compiler. The Xilinx XACT software was used to place and route the gate-level logic into the Xilinx FPGA.

4.3.3 Acquisition and Tracking Control

The receiver begins operation in acquisition mode. In this mode, the tracking loop is disabled, and the control logic searches for the proper phase of the PN sequence for despreading the received signal. The search process consists of allowing the demodulator to demodulate the incoming signal at a given code phase. The control logic checks for acquisition by monitoring the quality estimates from the demodulator, and, after enough samples, either accepting or rejecting the current code phase. If the current code phase is rejected, the control logic delays the phase of the local PN sequence by one-half chip ($T_c/2$) and checks for acquisition again. Once the phase of the local PN sequence is accepted, the control logic enables the tracking loop (the DLL described in Section 3.4.2) and switches to a tracking mode. During normal operation, should the quality estimates from the demodulator indicate loss of signal, the control module can switch back to acquisition mode and attempt to re-acquire the signal.

The acquisition and tracking control is implemented in the same FPGA as the demodulator. The control logic was described by VHDL code and synthesized along with the demodulator design. The tracking loop consists of the despreaders/downconverter modules presented earlier along with analog circuitry to calculate the difference in the outputs from the early and late branches. Once the signal strength difference between the early and late branches is found, additional analog circuitry provides filtering, gain, and voltage level adjustments to drive the control input of a voltage controlled crystal oscillator (VCXO). This VCXO provides the master clock that controls the despreading

and demodulator modules. Schematics of the circuit implementation are included in Appendix B.

4.3.4 Bit Handler

The bit handler block in Figure 4.4 is expanded in Figure 4.7. The bit handler module contains circuitry for making bit error measurements as well as providing data to the user. The test pattern generator duplicates the test pattern from the transmitter, and synchronization logic aligns the receiver test pattern with the incoming bit stream when the transmitter is sending the test pattern. A pulse is generated for every detected error, and a bit count signal is also provided. A microcontroller (not shown in the system block diagrams) activates the bit error test module and counts bits received and errors detected. The microcontroller interfaces with a notebook computer for collecting data on system performance. (The microcontroller is also used to configure the FPGA and receiver parameters.) Like the rest of the logic in the receiver, the bit handler is a VHDL design implemented in the Xilinx XC3064A FPGA.

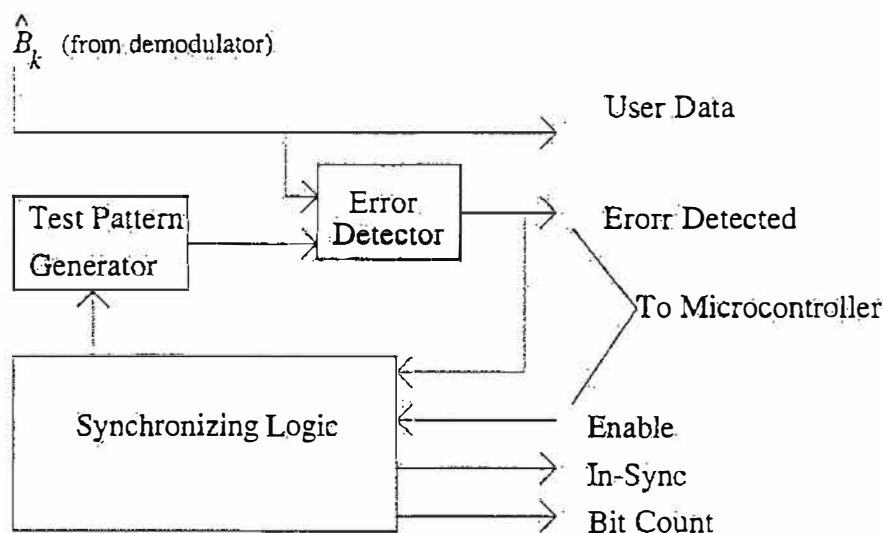


Figure 4.7 The Bit Handler Module.

4.4 Local Oscillator and Clock Designs

This project requires a number of stable timing sources for proper operation. The transmitter requires two main timing sources: a 915.000 MHz oscillator to provide the carrier signal for RF transmission and a chip clock for generating the PN spreading sequence. The receiver requires a 904.300 MHz oscillator for downconverting the received signal to 10.7 MHz, a 10.3 MHz oscillator for downconverting the 10.7 MHz signal to 400 kHz, and a voltage controlled crystal oscillator for generating the chip clock for the despreading sequence and operating the demodulator.

The 904.300 and 915.000 MHz oscillators are both implemented similarly. These oscillators are actually frequency synthesizers, generating the output signal from an oscillator that is phase locked to a crystal reference. As shown in Figure 4.8, these modules consist of a 904 or 915 MHz voltage controlled oscillator circuit built around the Motorola MC12149 VCO integrated circuit. This VCO is phase locked to a crystal reference with a Motorola MC145191 programmable phase-locked loop (PLL) chip. The configuration values used by the PLL are loaded from non-volatile memory (EEPROM) by a programming interface upon power-up. The programming interface also allows connection to a PC for reprogramming the EEPROM with different PLL settings. Thus, the 904.300 MHz and 915.000 MHz oscillators are essentially the same circuits with different configuration register values. Refer to the schematics in Appendix B for additional implementation details.

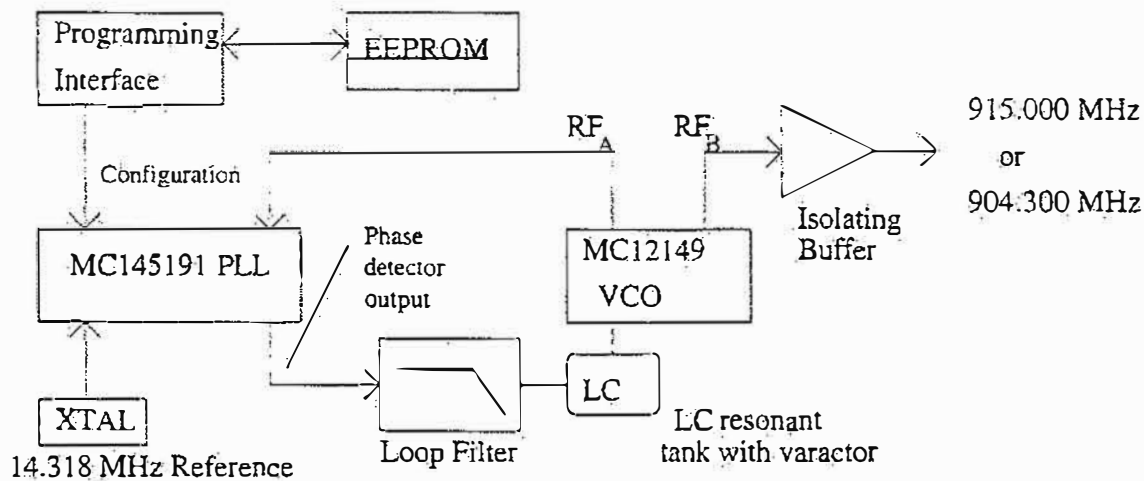


Figure 4.8 900 MHz Local Oscillator Block Diagram.

The chip clocks used by the transmitter and receiver are both generated from 25.6 MHz oscillators. A 25.6 MHz oscillator output is divided by two in the transmitter to generate the 12.8 MHz chip clock used for the spectral spreading sequence. In addition, the data bits are clocked into the transmitter by a bit clock generated by dividing the 12.8 MHz chip clock down to 100 kHz. The transmitter clock structure is shown in Figure 4.9.

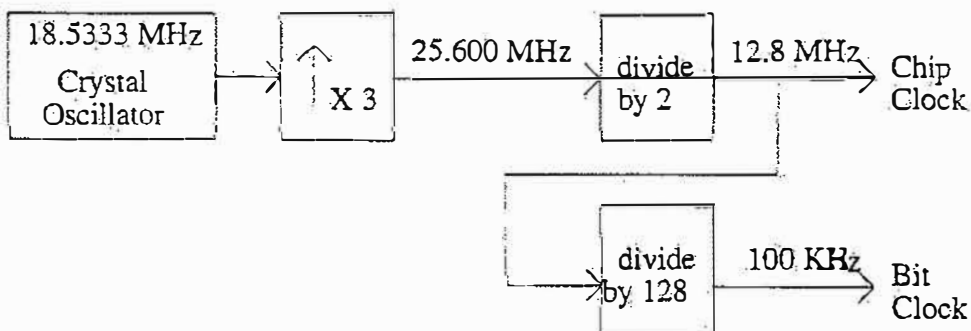


Figure 4.9 The Transmitter Clocks.

The clocks in the receiver are also based on a 25.6 MHz oscillator as shown in Figure 4.10. In the receiver, the 25.6 MHz clock is required for generating the despreading sequence because the control logic adjusts the receiver despreading sequence in steps of $T_c/2$ during acquisition mode; steps of $T_c/2$ require a clock running at twice the chip

rate -- that is, 25.6 MHz. In both the transmitter and receiver, the 25.6 MHz clocks are generated from the third harmonic of a 8.533333 MHz crystal oscillator with varactor tuning, resulting in the 25.6 MHz VCXO. The tuning voltage to the transmitter clock is set to a fixed value, but the tuning voltage to the receiver clock is the output of the code tracking loop (the delay lock loop). These VCXO circuits are included in the modulator and demodulator schematics in Appendix B.

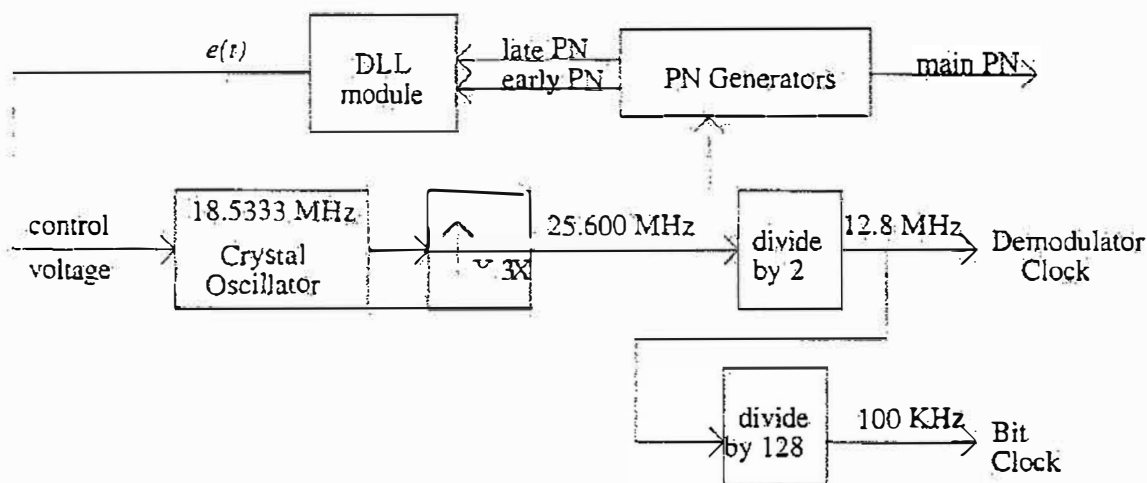


Figure 4.10 The Receiver Clocks.

The final oscillator required in the design is the 10.3 MHz local oscillator used to downconvert the 10.7 MHz IF to the final 400 kHz IF supplied to the demodulator. The 10.3 MHz output is generated from a 10.3 MHz crystal in a standard oscillator configuration. The schematic for the 10.3 MHz oscillator is included with the despreaders/downconverter schematic in Appendix B.

CHAPTER 5

SYSTEM PERFORMANCE

5.1 Transmitter Performance

The transmitter design described in Chapter 4 has been built and tested. The measured output power from the transmitter is 17.6 dBm. The output power spectrum with the random test data sequence input to the modulator is shown in Figure 5.1. To verify compliance with FCC Part 15 requirements, the transmitter spectrum was examined with a spectrum analyzer set to a 100 kHz resolution bandwidth (RBW). As shown in Figure 5.2, the peak signal level outside the 902-928 MHz band is 23.67 dB below the peak level within the band, meeting the out-of-band emissions limits. The peak power is about 3.5 dB at 915 MHz, meeting the maximum power spectral density limit of 8 dB. Figure 5.2 does show a significant carrier component at 915 MHz and spurious responses just inside the 902 and 928 MHz edges, but these levels are permissible.

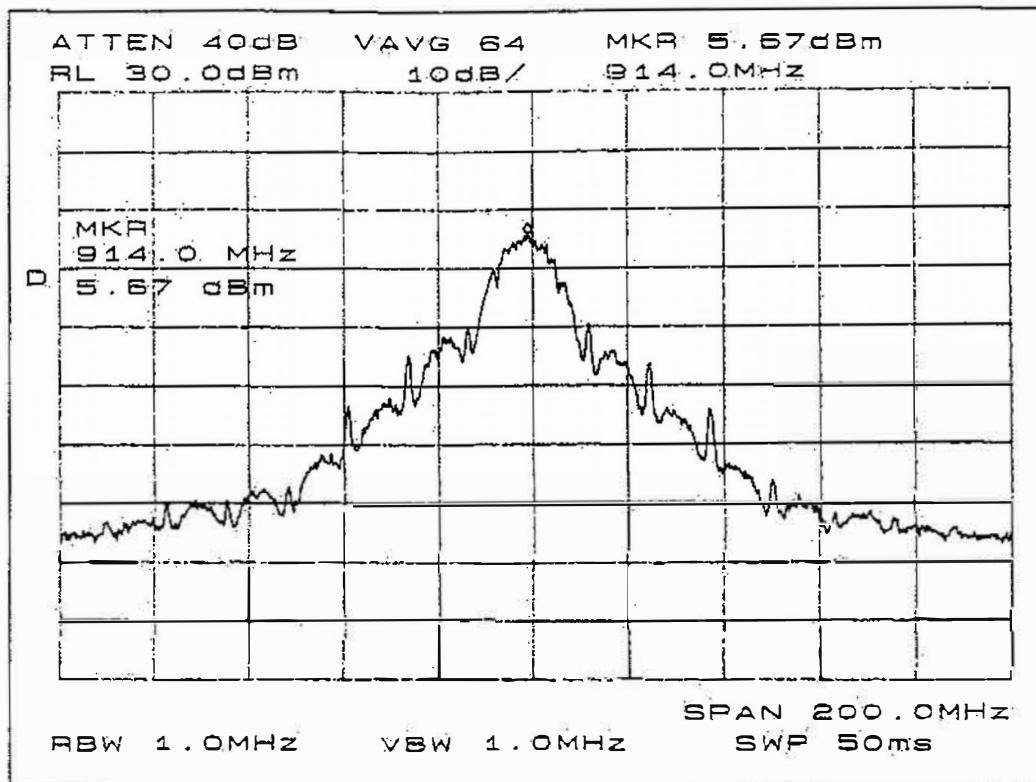


Figure 5.1 Spectrum of Transmitter Response at Wide Bandwidth.

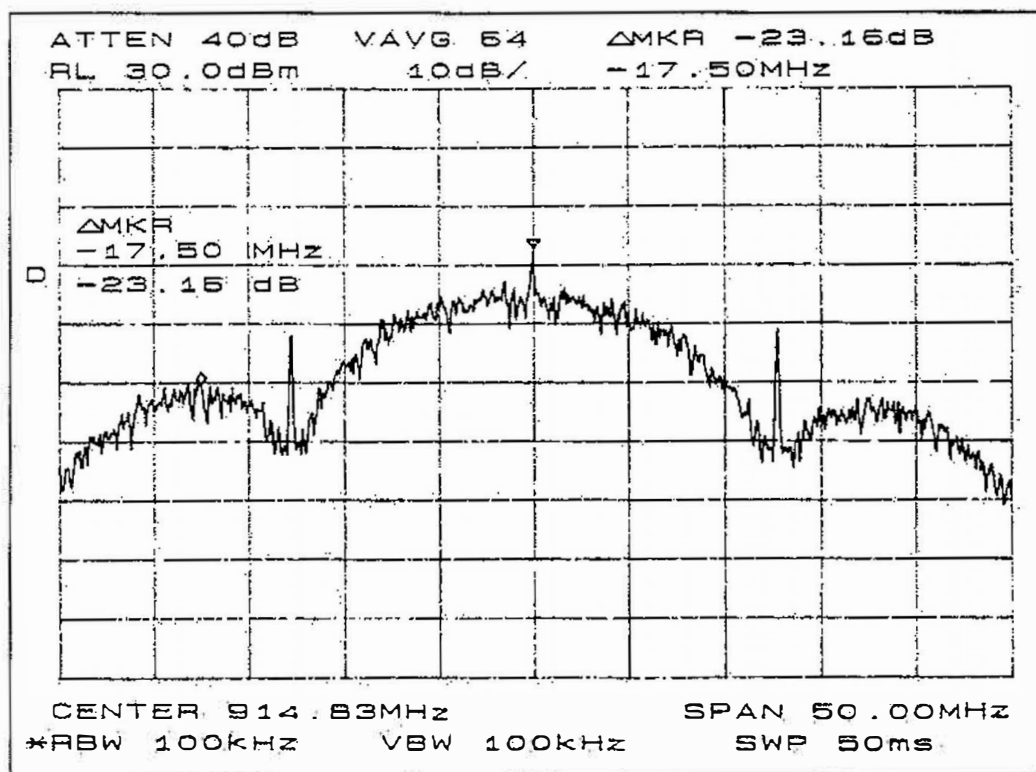


Figure 5.2 Spectrum of Transmitter Response at 100 kHz RBW.

5.2 Receiver Performance

Using the transmitter described above as a signal source, the performance of the receiver was measured at different power levels. The test setup shown in Figure 5.3 was used for measuring receiver performance.

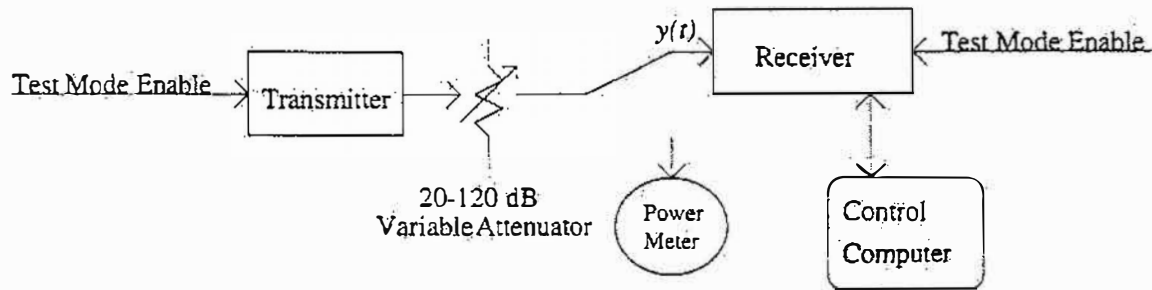


Figure 5.3 The Receiver Test Setup.

To calibrate the test setup shown in Figure 5.3, the receiver is temporarily disconnected, and the power meter is connected in its place to measure the signal strength at $y(t)$. The variable attenuator is set to 20 dB, and the transmitter power is measured with an HP438A RF power meter. Once an initial power reading is made, the attenuator settings can be varied to provide a calibrated power sweep to characterize receiver performance.

Under the test setup, the receiver was found to acquire the spread spectrum signal at an input power level of -109 dBm and operate with a bit error rate of 10^{-6} at an input power level of -99 dBm. The measured bit error rate vs. input power level for the receiver is shown in Figure 5.4. The receiver performed quite well, coming to within 6.5 dB of the performance of an ideal DBPSK system, based on the calculations in Appendix A.

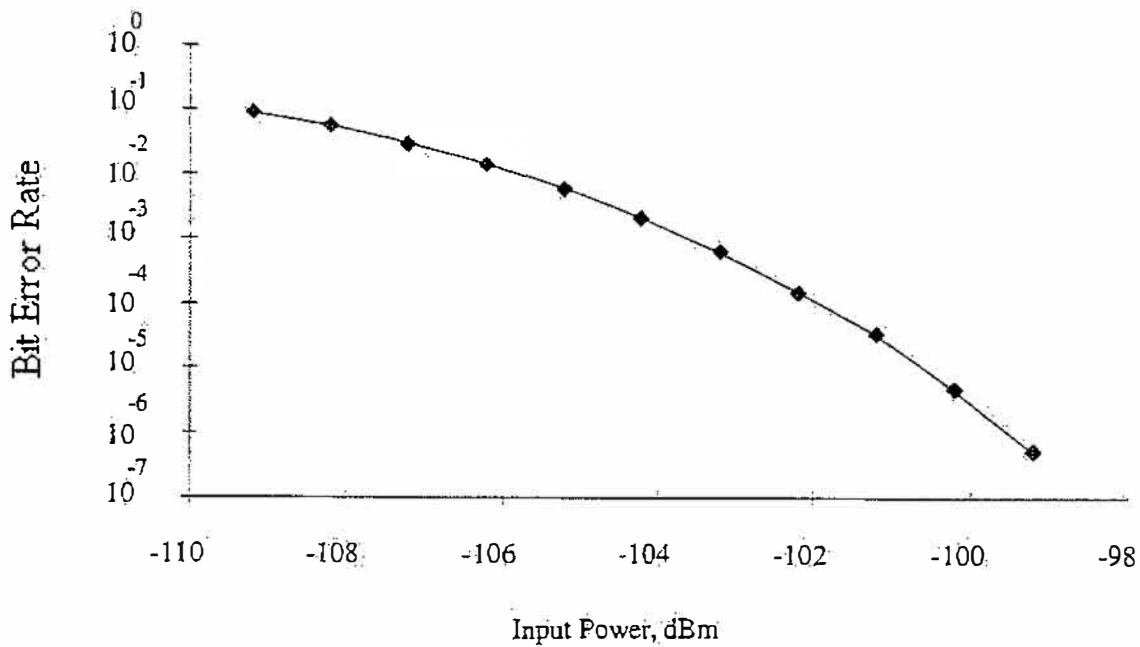


Figure 5.4 Receiver Performance.

The transmitter and receiver were then separated, and performance was measured for outdoor and indoor conditions. For outdoor measurements, the receiver was positioned several yards from any obstacles. The transmitter was then positioned at various points from 600 to 1050 feet from the receiver. The receiver performance was measured at each location, and the results are plotted in Figure 5.5.

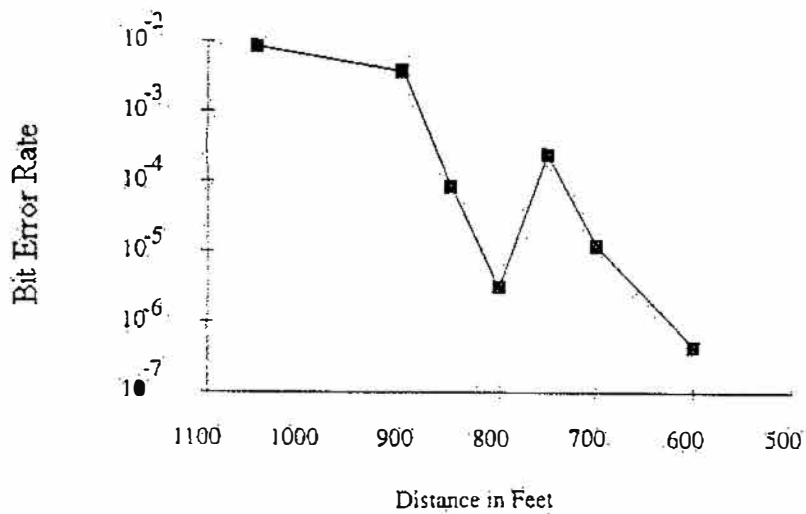


Figure 5.5 Outdoor Performance.

For indoor measurements, the location of the receiver was fixed and the transmitter was moved. The receiver antenna was placed on the top of a five-foot high office partition wall (cubicle wall). The transmitter was moved around the office area, and the receiver performance was monitored. The receiver operated with a probability of bit error less than 10^{-7} throughout the office environment. The maximum distance tested in the office environment was about 62 feet due to space limitations. Additional indoor measurements were made in a long hallway; a probability of bit error of about 10^{-5} was measured around 300 feet, and about 10^{-4} at 400 feet.

CHAPTER 6

CONCLUSIONS

This project consisted of the design and implementation of a direct sequence spread spectrum wireless modem. This modem has been built and tested, and the system performance met the project goals. The measurements presented in Chapter 5 show that the system met the requirements for operation in the unlicensed ISM band at 902-928 MHz. Testing also shows that the radio modem achieved the performance objectives, operating over 400 feet indoors and over 500 feet in an outdoor environment. The system has been used successfully to transmit asynchronous RS-232 data at 38,400 bits per second, and the built-in test sequence has verified operation at 100,000 bits per second.

While this direct sequence spread spectrum modem met the design objectives, there are a number of enhancements, both in terms of features and performance, that could be considered for future work. Useful additional features would be to provide bidirectional data transfer and to support multiple links in the same area (multiple access). Multiple spreading codes could be used to provide these enhancements, or time-division switching techniques (time division duplex and time division multiple access) could be considered. Adding these additional features would also require considering data transmission protocols and might increase the need for error correcting codes.

The performance of the system could also be enhanced in several ways. The 915 MHz frequency synthesizers used in the transmitter and receiver exhibit fairly high phase noise and low long-term stability. Improving the frequency synthesizers would result in a cleaner signal being transmitted as well as less noise being added to the incoming signal in the receiver. In addition, a more advanced demodulator could be implemented if additional logic circuitry were utilized. The existing differentially coherent demodulator could be enhanced, or a coherent demodulator (with automatic frequency correction) could be implemented. A third enhancement to the system would be to add channel coding, thereby reducing the number of errors seen by a user.

Despite its relative simplicity, the system implemented in this project demonstrates all the basic aspects of a spread spectrum radio, including modulation, spreading, acquisition, tracking, and demodulation; it is a fully functional radio modem operating in the 902-928 MHz ISM band.

APPENDIX A

LINK BUDGET ANALYSIS

The determination of signal and noise power levels throughout a communication system is called *link budget analysis*, and the goal of the analysis is to determine performance requirements and constraints for the transmitter and receiver. For this project, the receiver design will be chosen to limit complexity, and the transmitter power will be determined to meet the system objectives. Thus, the link budget analysis will be used to determine the minimum transmitter output power.

Throughout this analysis, all power quantities will be expressed in decibel-milliwatts (dBm), and system gain or losses will be expressed in decibels (dB). Using this convention, the transmitter power needed, P_t , is related to the receiver sensitivity, R_{sen} , and the path loss, L_{path} , by

$$P_t \geq R_{sen} + L_{path}. \quad (A.1)$$

The receiver sensitivity R_{sen} is the input power level at which the system performance meets a specified goal. The receiver sensitivity can be approximated from the demodulator characteristics, the antenna input noise power, and the noise characteristics of the receiver. The demodulator is characterized by the bit energy to noise ratio, E_b / N_0 ,

at which a given probability of bit error is realized. The noise characteristics of the receiver sections are combined into a single noise figure N_f , and the antenna input noise power is represented as P_n . Using these terms, the receiver sensitivity can be expressed as

$$R_{sen} = \frac{E_b}{N_0} + N_f + P_n. \quad (A.2)$$

The value for E_b / N_0 depends on the demodulator type and desired level of performance.

For an average bit error rate of 1 in 10^6 , an ideal DBPSK demodulator requires

$$E_b / N_0 = 11 \text{ dB} \text{ [5]}.$$

The value for N_f depends on the input structure of the receiver. The receiver structure shown in the schematics in Appendix B is designed to have a noise figure of 3.8 dB; for purposes of the link budget analysis, additional margin will be added, and a value of 5 dB will be used for N_f .

The antenna noise power depends on thermal noise in the environment as well as sources of interfering signals. Neglecting any sources of interference (in keeping with the assumption of AWGN), the input noise power for the receiver is given by [15] as

$$P_n = kT_a B_n, \quad (A.3)$$

In (A.3), k is Boltzmann's constant (1.38×10^{-23} J/K), T_a is the antenna temperature (assumed to be 270 K), and B_n is the noise bandwidth of the receiver (approximated by 200 kHz for 100 kbps with BPSK modulation). Evaluating (A.3) gives $P_n = -121.3 \text{ dBm}$.

Using $E_b / N_0 = 11 \text{ dB}$, $N_f = 5 \text{ dB}$, and $P_n = -121.3 \text{ dBm}$ and evaluating (A.2) give

$$R_{sens} = -121.3 + 5 + 11 = -105.3 \text{ dBm}. \quad (A.4)$$

Accordingly, the receiver will need an input power level of about -105 dBm minimum to meet the desired probability of bit error.

Given the sensitivity of the receiver, the next step to finding the minimum transmitter power is to determine the signal strength degradation experienced through the channel. For isotropic antennas in a line-of-sight environment, the path loss can be estimated as [16].

$$L_{path} = 32.4 + 20 \log(D_{km}) + 20 \log(F_{MHz}). \quad (A.5)$$

For a distance of 500 ft (0.15 km) ($D_{km} = 0.15$) at 915 MHz ($F_{MHz} = 915$), (A.5) gives $L_{path} = 75.3$ dB for isotropic antennas. The transmitter and receiver in this project will be equipped with quarter-wave monopole antennas with a gain of 6 dB each. This antenna gain will reduce the path loss by a total of 12 dB, giving a final $L_{path} = 63.3$ dB.

Evaluating (A.1) with the values for R_{sens} and L_{path} establishes a lower bound on the transmitter power as

$$P_t \geq -105.5 + 63.3 = -42.2 \text{ dBm}. \quad (A.6)$$

This analysis establishes a theoretical lower bound on the power requirements of the transmitter to be -42.2 dBm. In practice, the path loss may be much higher due to absorption and reflection of the signal by nearby objects and the ground. In addition, the signal may be subjected to fading and/or multipath propagation effects, both of which can seriously limit the performance of a simple receiver. (See [5] for more information on radio wave propagation in the 800-1000 MHz range, and [4] for a study on indoor radio channels.) As a result of the concern for possible additional signal degradation, the transmitter power will be set to at least 10 dBm, allowing a large margin.

APPENDIX B

SCHEMATIC DIAGRAMS

This appendix presents the complete schematics for the spread spectrum modem developed in this project. When designing 900 MHz circuits, care must be taken to minimize stray inductance and capacitance effects throughout the circuit. As a result, all of these circuits were constructed on printed circuit boards using surface mount components and careful layout considerations. The schematics indicate several particularly sensitive areas where bypassing capacitors or other layout items are critical. In addition to using careful construction techniques, most of the circuits were enclosed in tightly sealed aluminum boxes to provide isolation from other sections of the circuit. The 900 MHz oscillators used in the transmitter and receiver RF sections are extremely sensitive to external disturbances, and were very carefully shielded.

The receiver schematics are shown in Figure B.1, the transmitter schematics in Figure B.2, and the frequency synthesizer schematics in Figure B.3. In addition to the electrical details shown in the schematics, the design contains several programmable devices. Routine digital design techniques were used to implement the modulator, demodulator, and control circuits in FPGAs, and the control programs for the microcontrollers included in the transmitter and receiver are fairly basic. Since these portions of the design are straightforward, they are not included in this appendix.

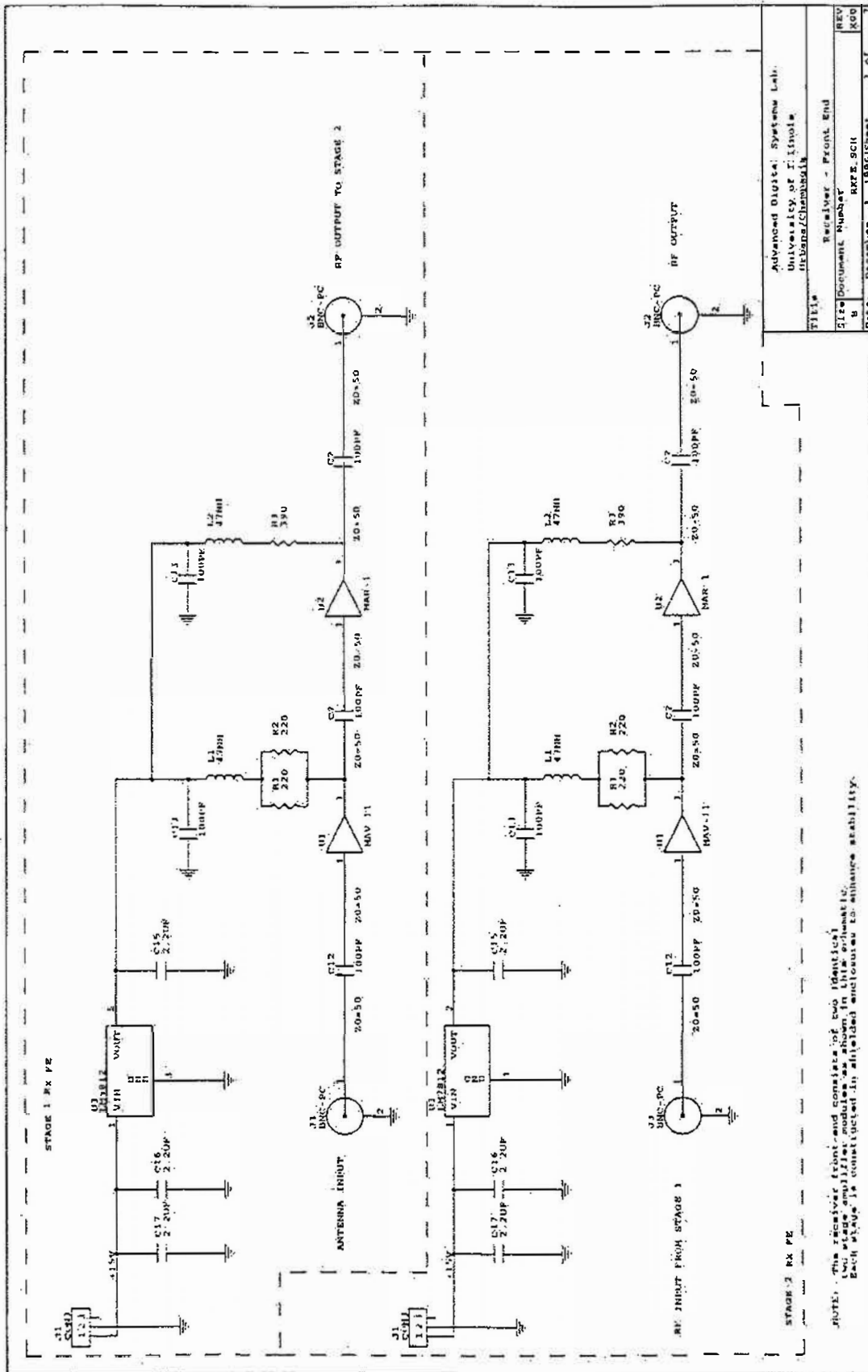


Figure B.1. Receiver Schematics.

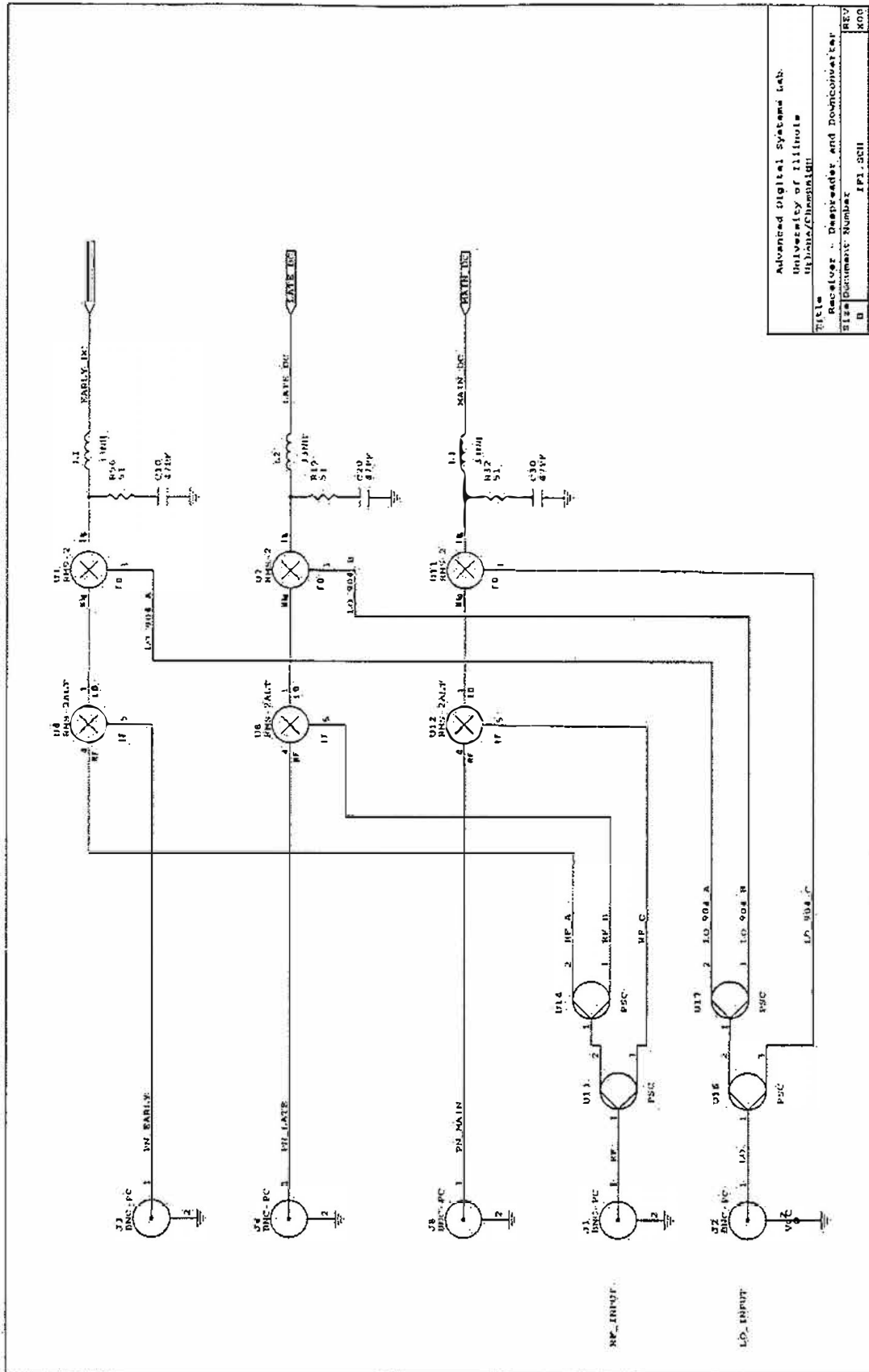


Figure B.1 Receiver Schematics (cont.)

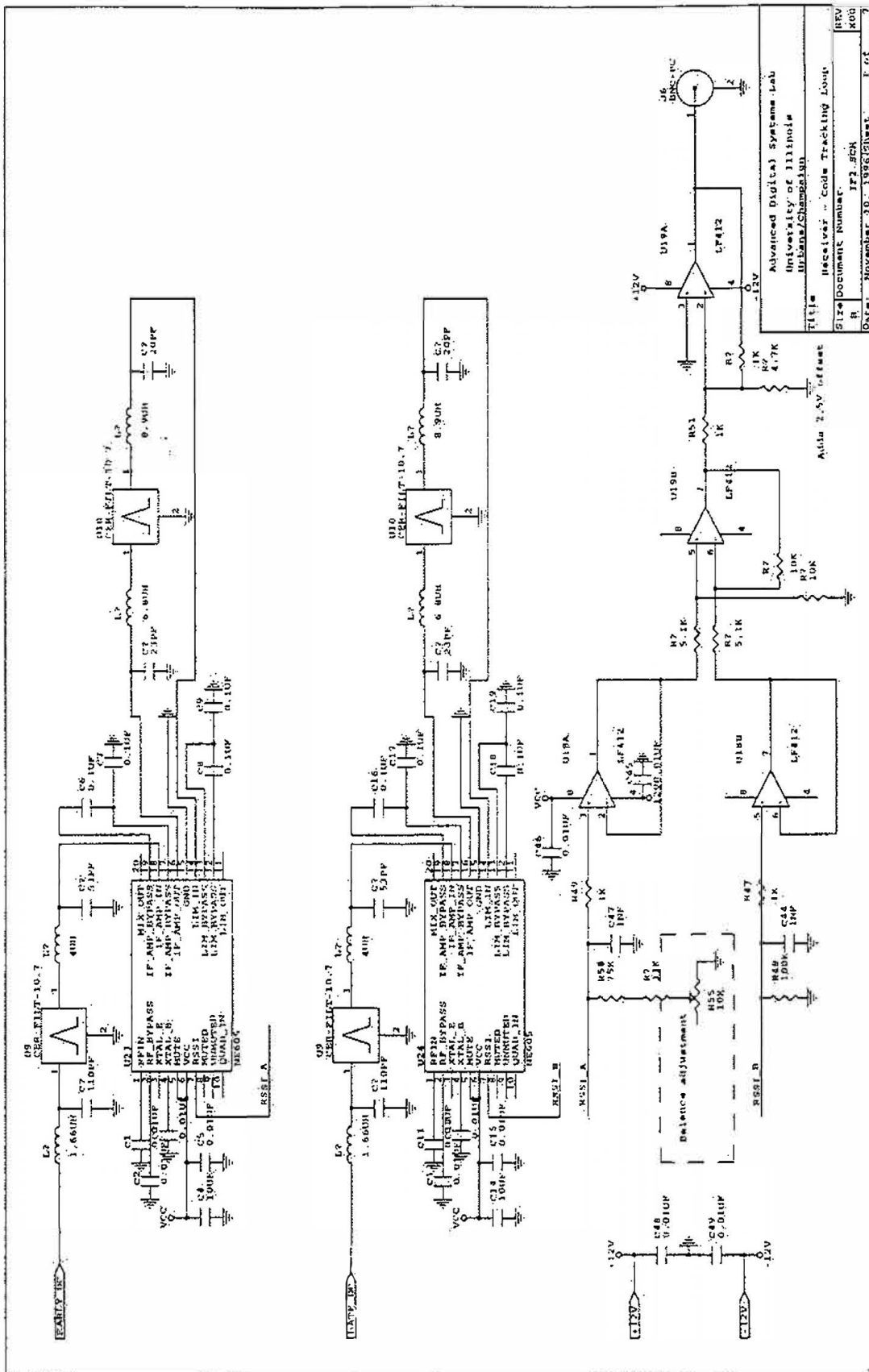


Figure B.1 Receiver Schematics (cont.)

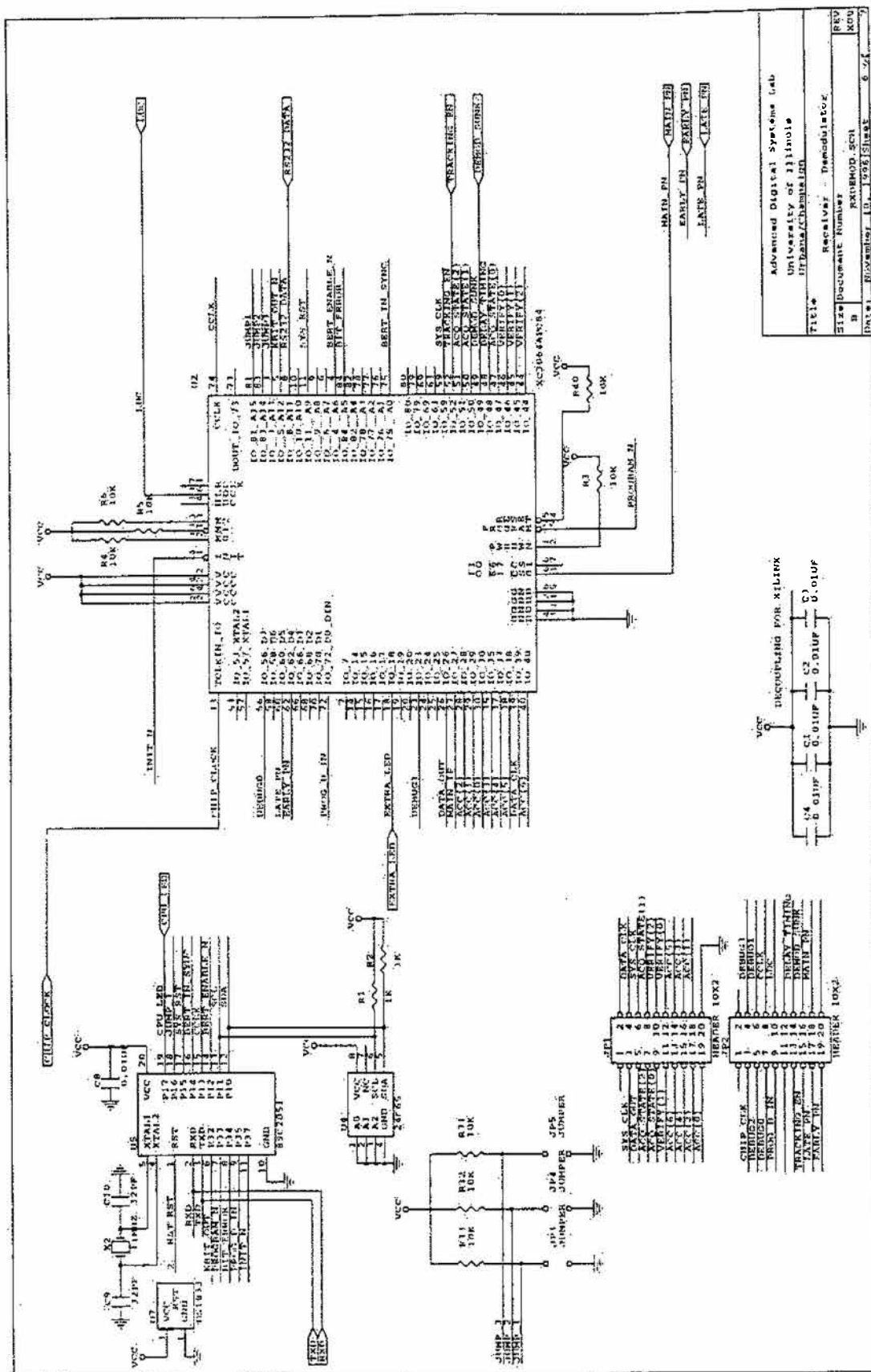


Figure B.1 Receiver Schematics (cont.)

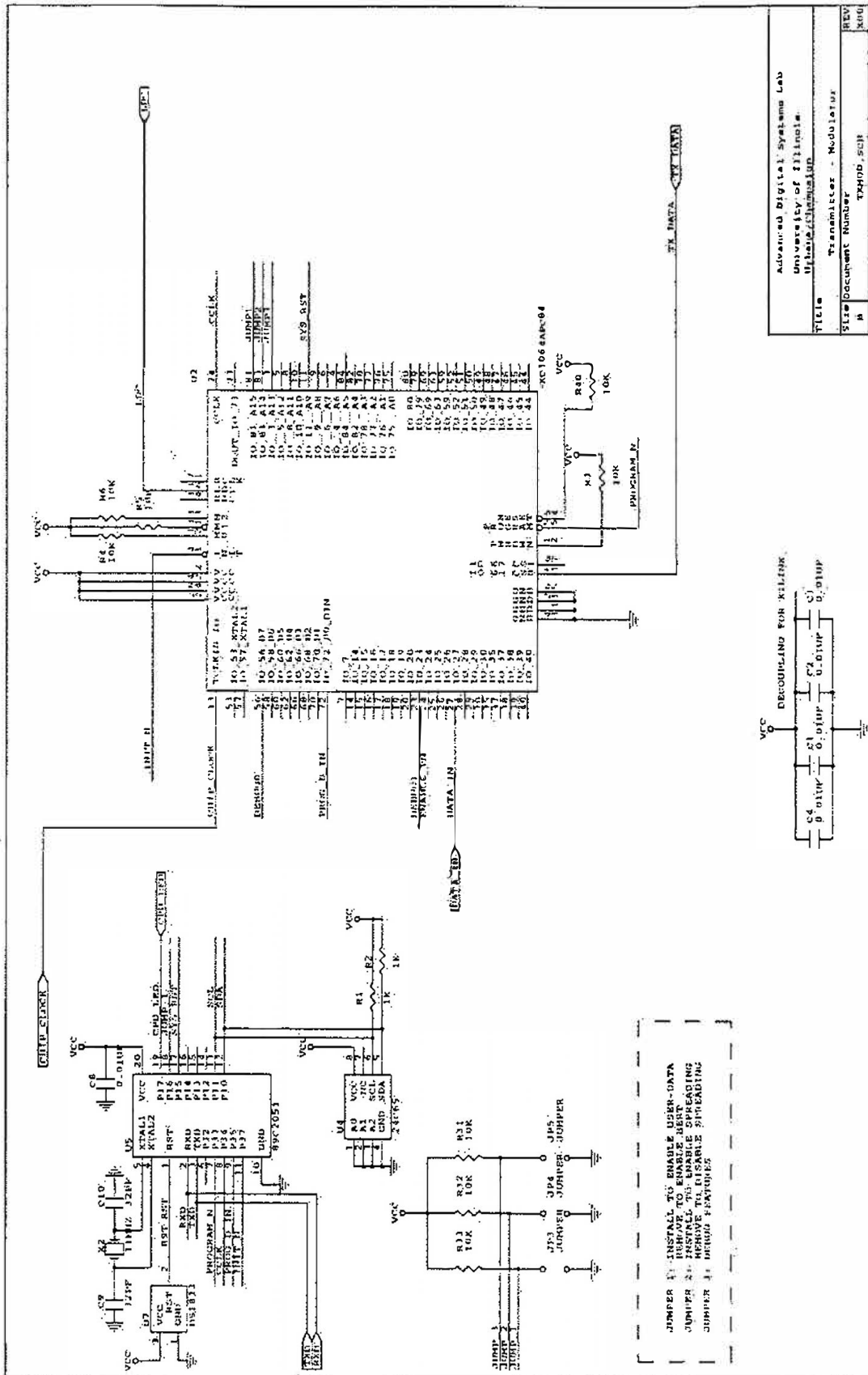


Figure B.2 Transmitter Schematics (conf.)

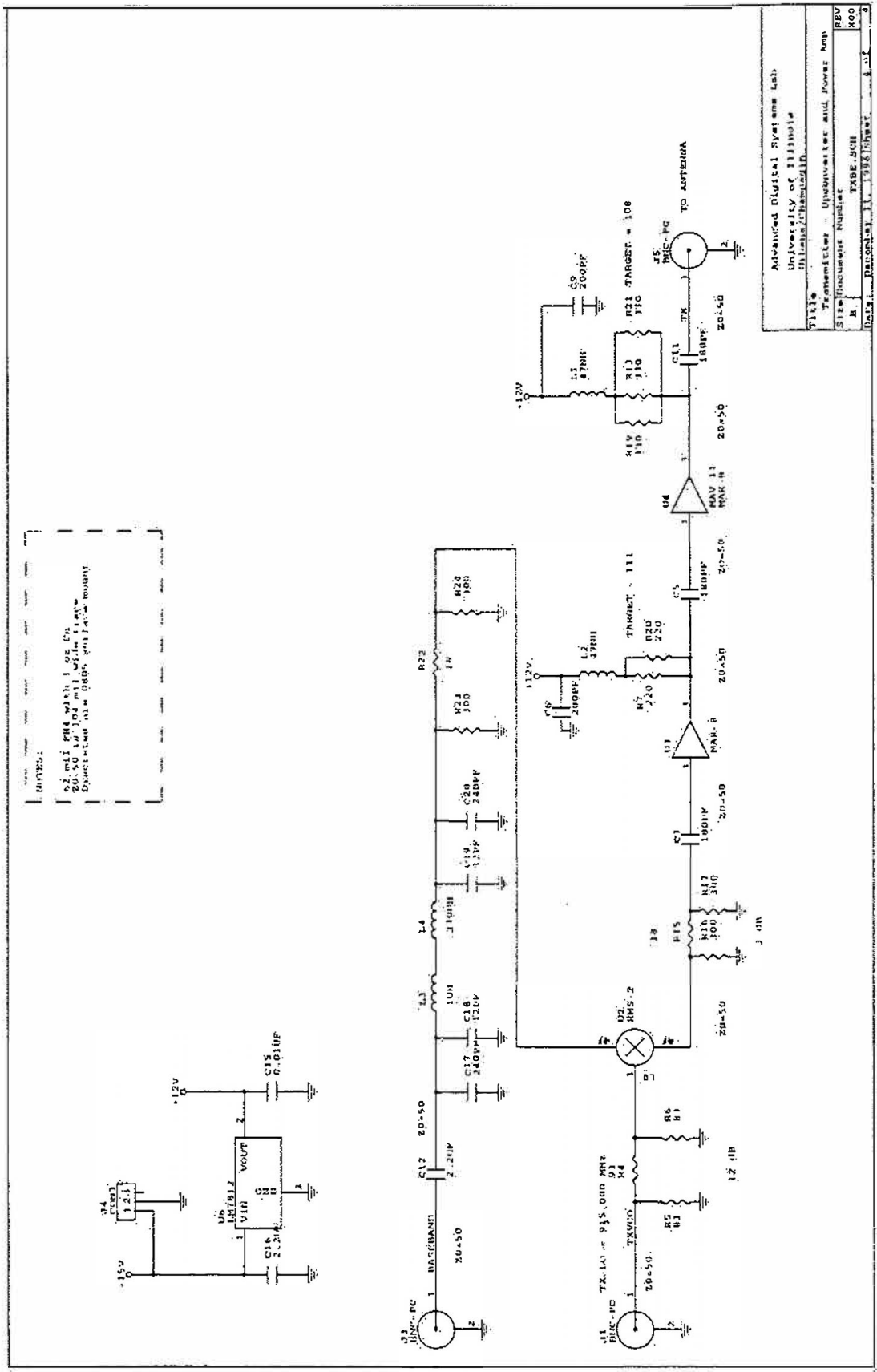


Figure B.2 Transmitter Schematics (cont.)

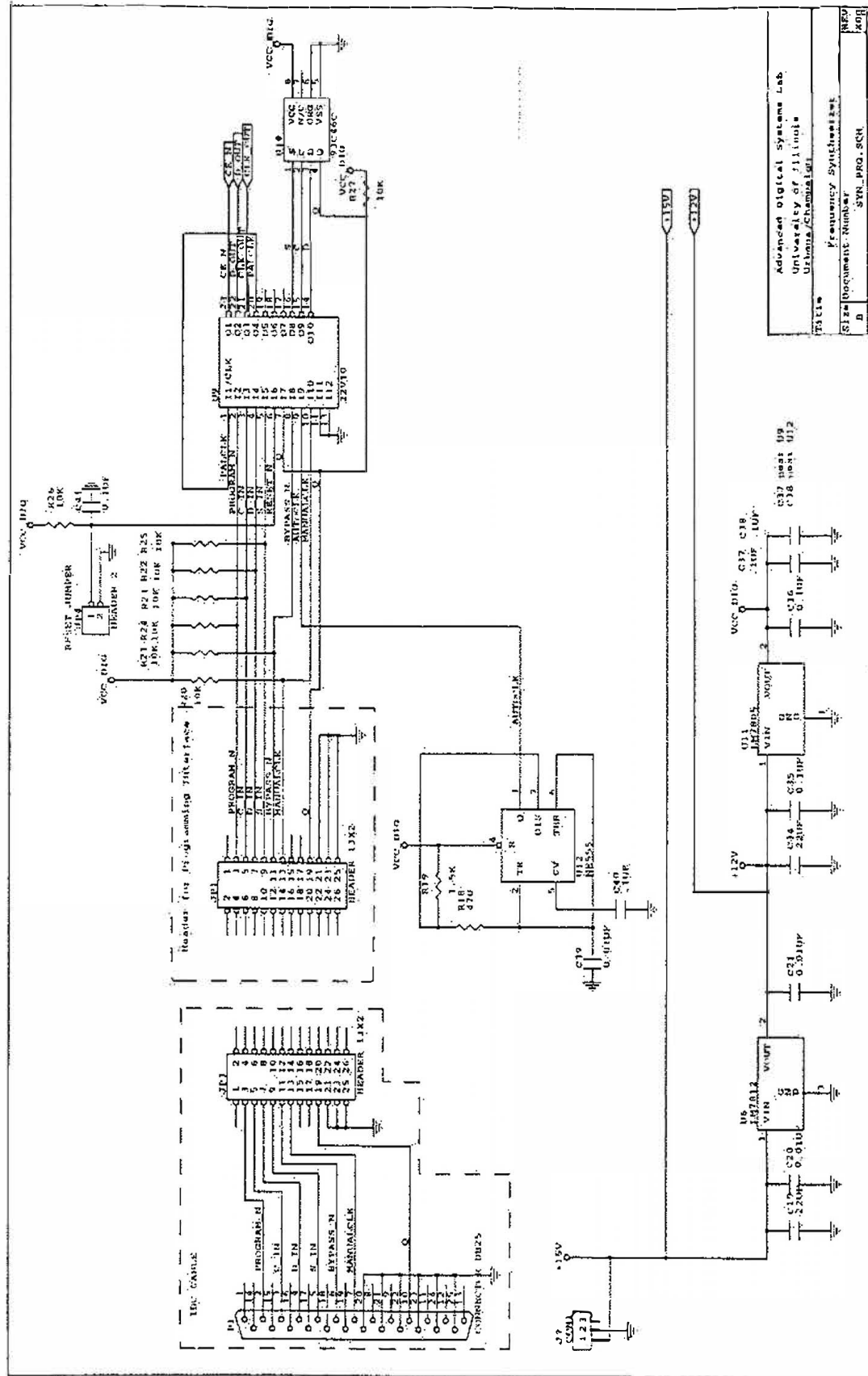


Figure B.3 Frequency Synthesizer Schematics.

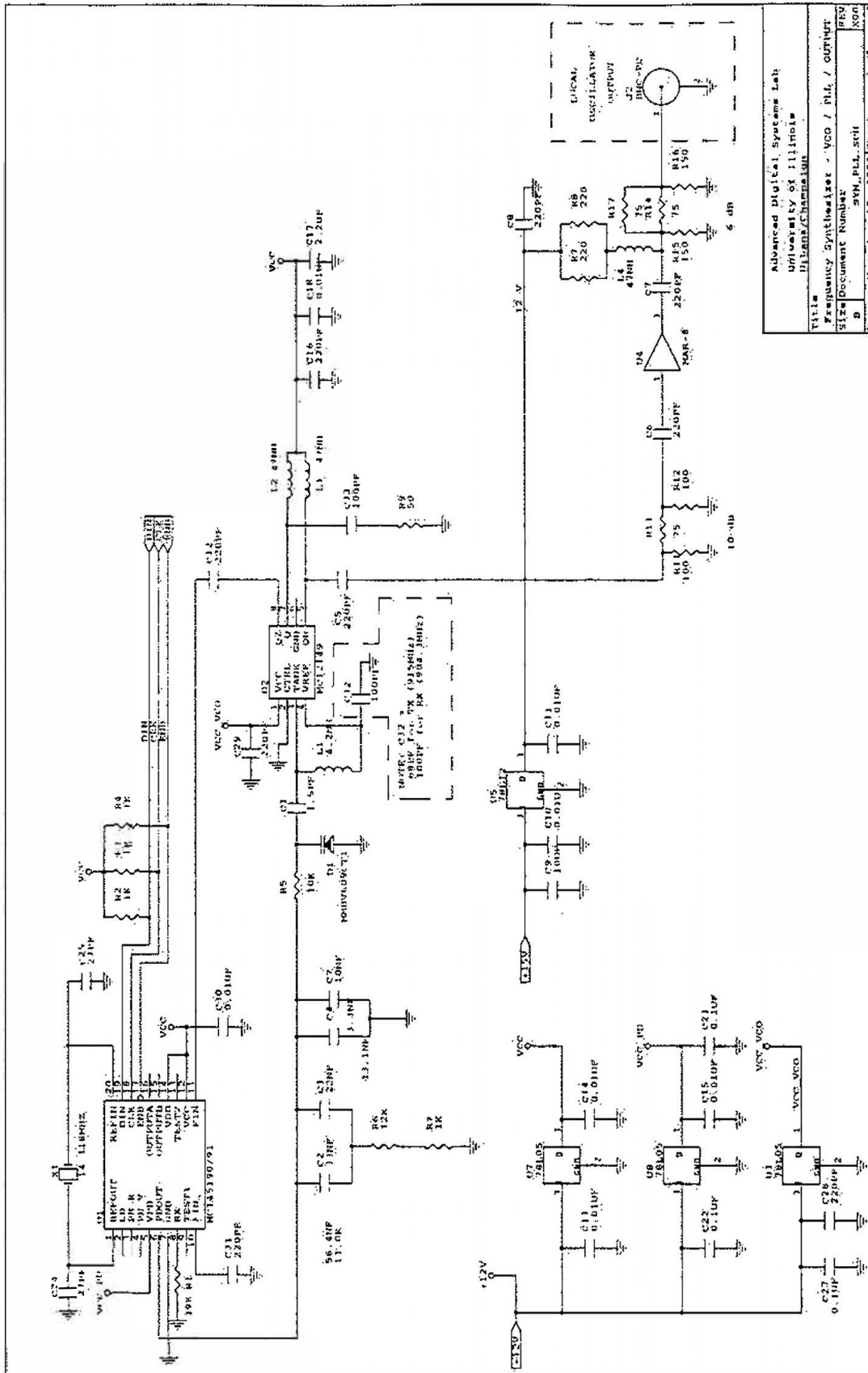


Figure B.3 Frequency Synthesizer Schematics (cont.)

APPENDIX C

RADIO DESIGN CONSIDERATIONS

During the course of this project, several areas of the design proved to be especially challenging. This appendix provides a summary of some of the key challenges in the design of a spread spectrum digital radio system. Critical design items are listed below by subject.

Oscillators

- The RF oscillators for the transmitter and receiver are critical elements in the radio. To obtain any reasonable level of frequency stability, the RF oscillator must be locked to a crystal reference.
- The RF oscillators will also be sensitive to injection locking; this occurs when the oscillator frequency is pulled towards any incoming signal at a nearby frequency. An early design for the project that attempted to convert the received signal directly from RF to baseband was unsuccessful because a medium- or high-level received signal would distort the receiver's local oscillator through injection locking. The local oscillator in the transmitter required careful shielding so that it did not injection-lock to the transmitted signal. The design of the oscillator should provide as much reverse-path isolation as possible, shielding the oscillator circuit from any noise or loading effects at its output.

Choice of LO Frequencies

- No local oscillator (LO) frequencies (or harmonics) should lie in the passband of the receiver front end. Even with spread spectrum systems, a high-level local oscillator signal can interfere with the operation of the system if any of the LO signal leaks onto the receiver's antenna.

Multiple IF Sections

- As mentioned above, an early attempt at a single conversion receiver was unsuccessful due to injection-locking problems in the receiver local oscillator. Even if that problem had been avoided, a multiple IF (intermediate frequency) design would probably have been needed. The high level of amplification needed to demodulate the lowest level input signals would likely cause stability problems if all of the gain were placed at a single frequency. In addition, it might be necessary to use additional IFs to avoid placing a LO in the receiver's passband. In this project, the receiver circuits required careful shielding to prevent excessive leakage of the LO onto the antenna. (The 904,300 MHz LO was interfering with the system since the modem was designed to receive the whole 902-928 MHz band.)

Circuit Construction Techniques

- As mentioned in Appendix B, circuits at 900 MHz must be built carefully. Grounding is a key issue when laying out the printed circuit boards. It is especially important to use plenty of vias to tie the top and bottom ground places together. Tightly-coupled top and bottom ground planes are critical near the ground leads of the high-gain amplifier integrated circuits -- the ground leads must be "staked" to both sides of the circuit board as near to the ground leads as possible.
- Careful shielding is essential for the high-gain amplifier and oscillator circuits.

Demodulator Design Considerations

- A demodulator for a hard-limited IF signal must over-sample the IF signal at a very high rate to obtain sufficient phase resolution for effective demodulation. The demodulator used in this project over-sampled at 32 times the IF frequency, and testing showed that a lower rate significantly reduced system performance.
- The (differentially) coherent demodulator must provide for frequency correction of the received signal. Even with precision crystal references accurate to 1 part in 10^6 , the frequency error at 915 MHz can degrade demodulator performance if some means of compensation is not provided.

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